



# SKM-U

Rev : 1.1

ECS  
CONFIDENTIAL

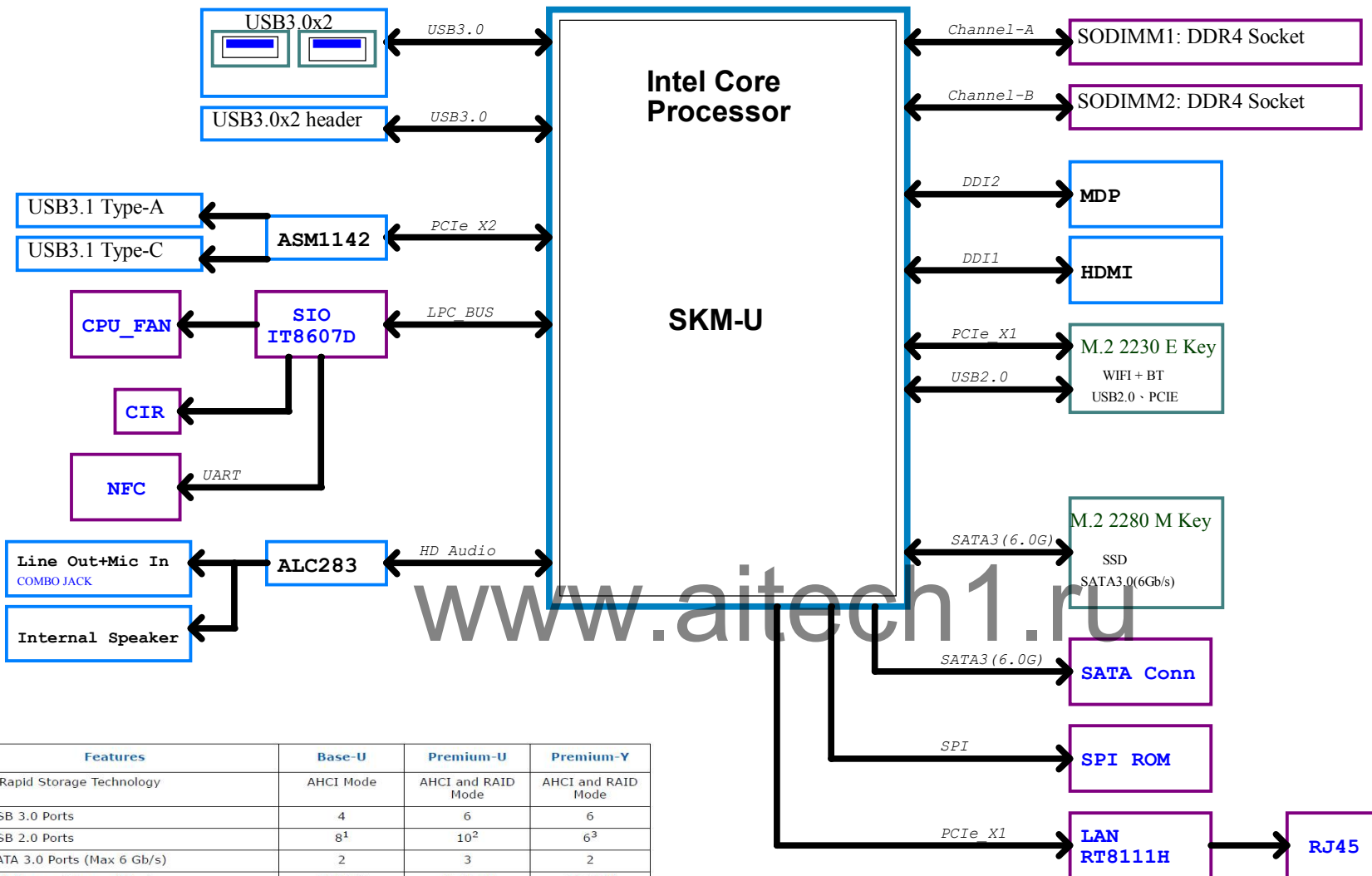
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## REVISION HISTORY:

Rev	Date	Notes
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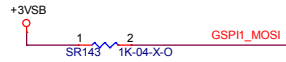
Features	Base-U	Premium-U	Premium-Y
Intel® Rapid Storage Technology	AHCI Mode	AHCI and RAID Mode	AHCI and RAID Mode
Total USB 3.0 Ports	4	6	6
Total USB 2.0 Ports	8 <sup>1</sup>	10 <sup>2</sup>	6 <sup>3</sup>
Total SATA 3.0 Ports (Max 6 Gb/s)	2	3	2
Total PCI Express* Lanes (Gen)	10 (2.0)	12 (3.0)	10 (3.0)
Total Intel® RST capable PCIe and SATA Express <sup>4</sup> Storage Devices	0	2 <sup>5</sup>	2 <sup>5</sup>

Features	Base-U	Premium-U	Premium-Y
<b>Notes:</b> 1. USB 2.0 port numbers: 1-8 2. USB 2.0 port numbers: 1-10 3. USB 2.0 port numbers: 1-6 4. SATA Express Capable Ports (x2) 5. Intel® RST PCIe supports RAID configuration 0/1			

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

HDMI

mDP



Boot Device Select:

BOOT DEVICE	GSPI1_MOSI
SPI	0
LPC	1

GSPI1\_MOSI internal pull-down

Strap Pin Select:

Strap Pin	GPP_B18
No Reboot (DI)	0
No Reboot (EN)	1

GPP\_B18 internal pull-down

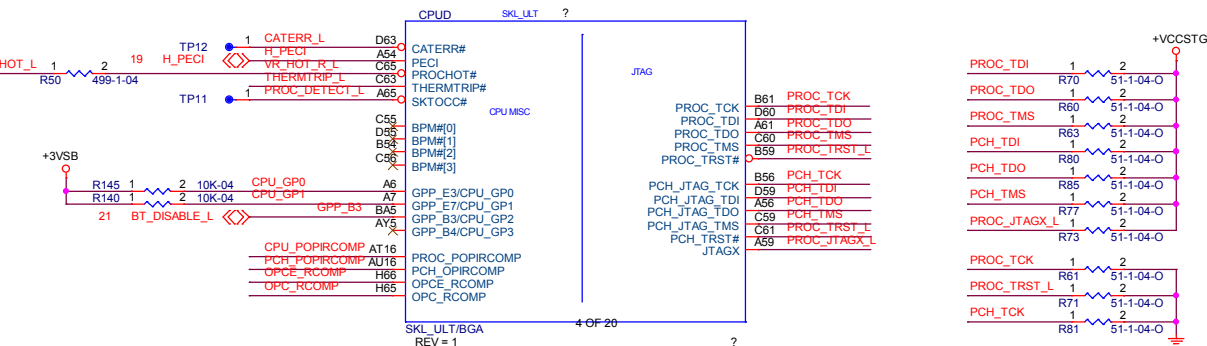
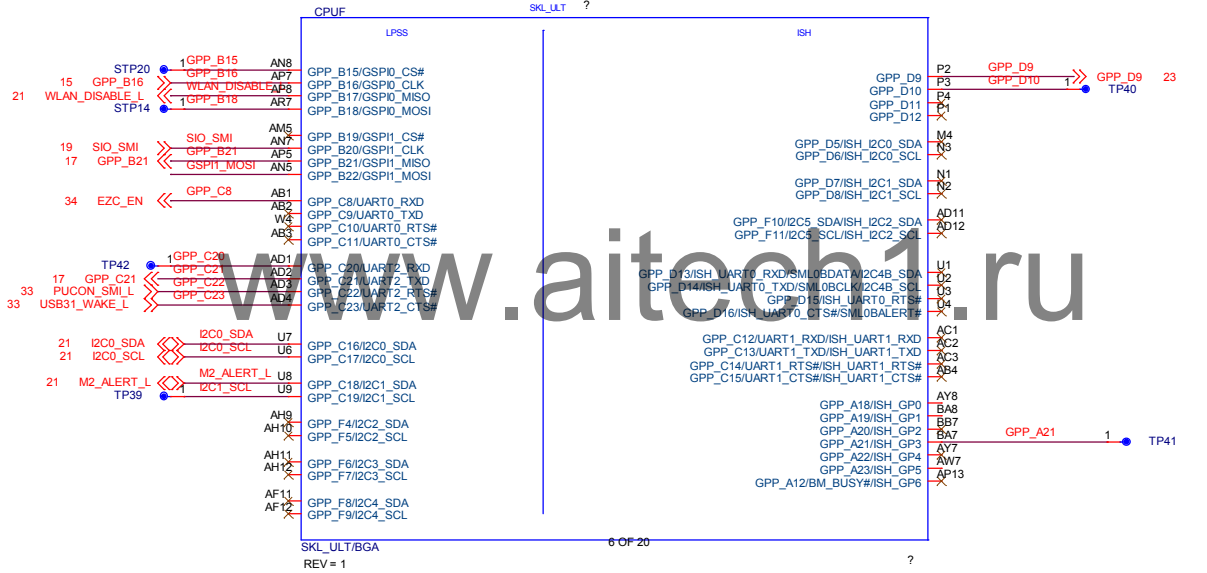
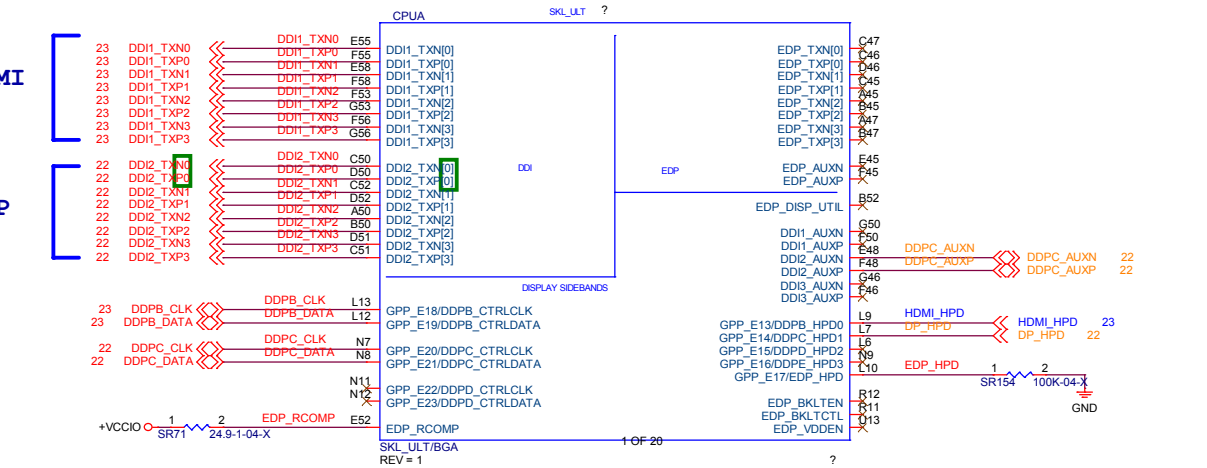
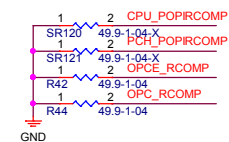
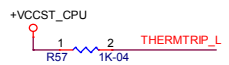
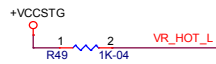
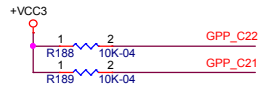
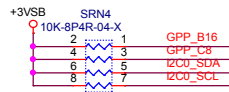
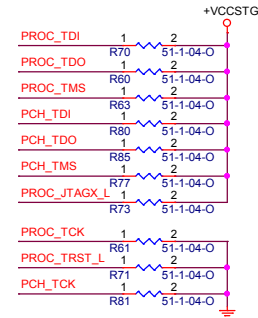
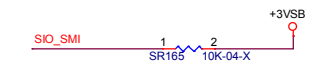
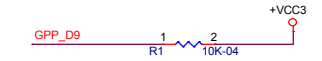


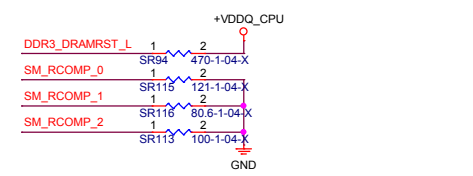
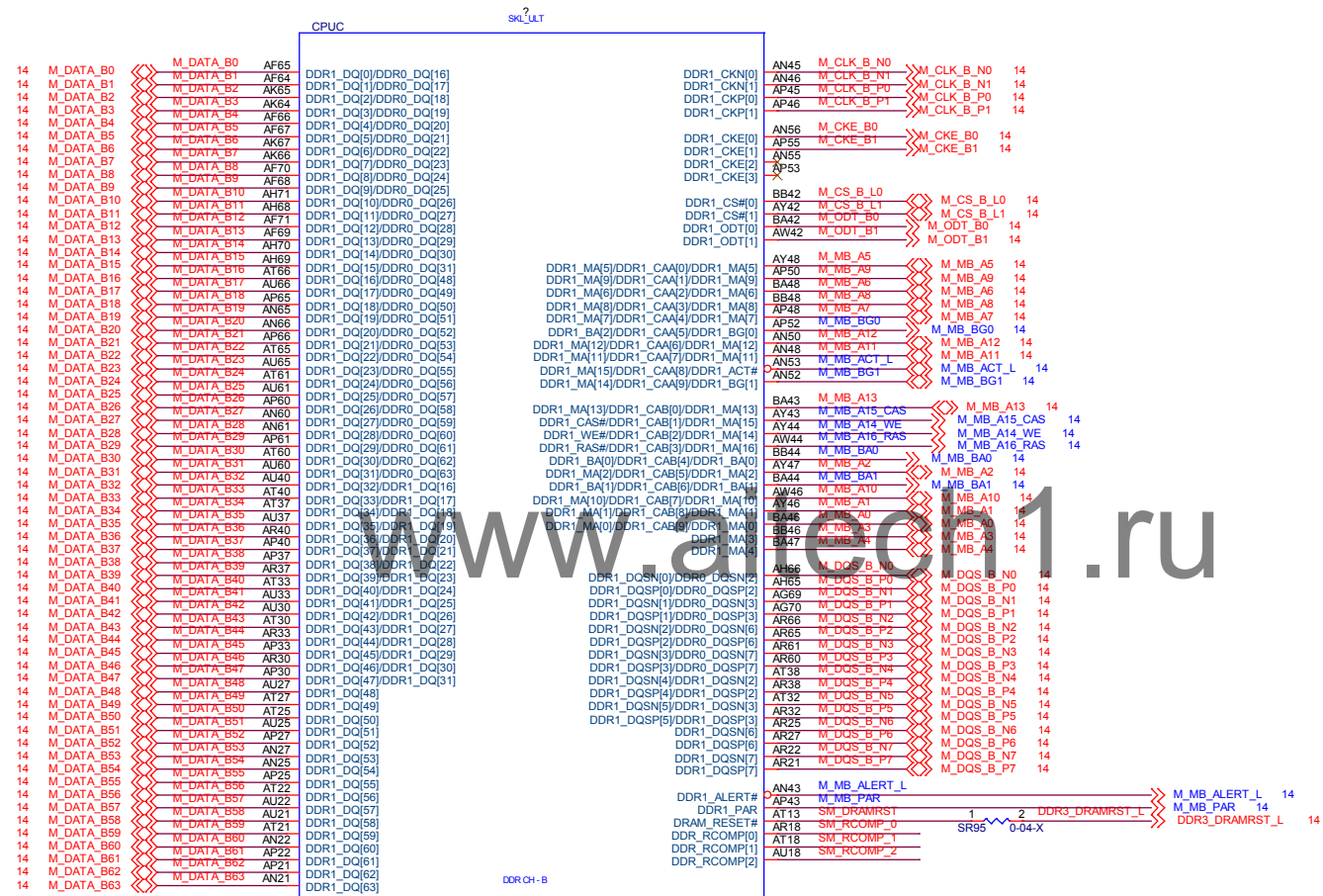
Table 7-1. Mapping of HDMI\* Signals for DDI Ports

Port	Digital Display Interface Plus	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMI1_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMI1_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMI1_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMI1_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMI1_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMI1_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMI1_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMI1_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CLK
Port 2	DDI2_TXP[0]	DDI2_LANE0_DP	HDMI2_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMI2_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMI2_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMI2_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMI2_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMI2_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMI2_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMI2_CLK_DN
	Hot plug detect used by HDMI Port 2	DDPC_HPD	DDI2_HPD_Q
	HDMI DDC lines for Port 2	DDPC_CTRLCLK	DDI2_CTRL_CLK



**Elitegroup Computer Systems**





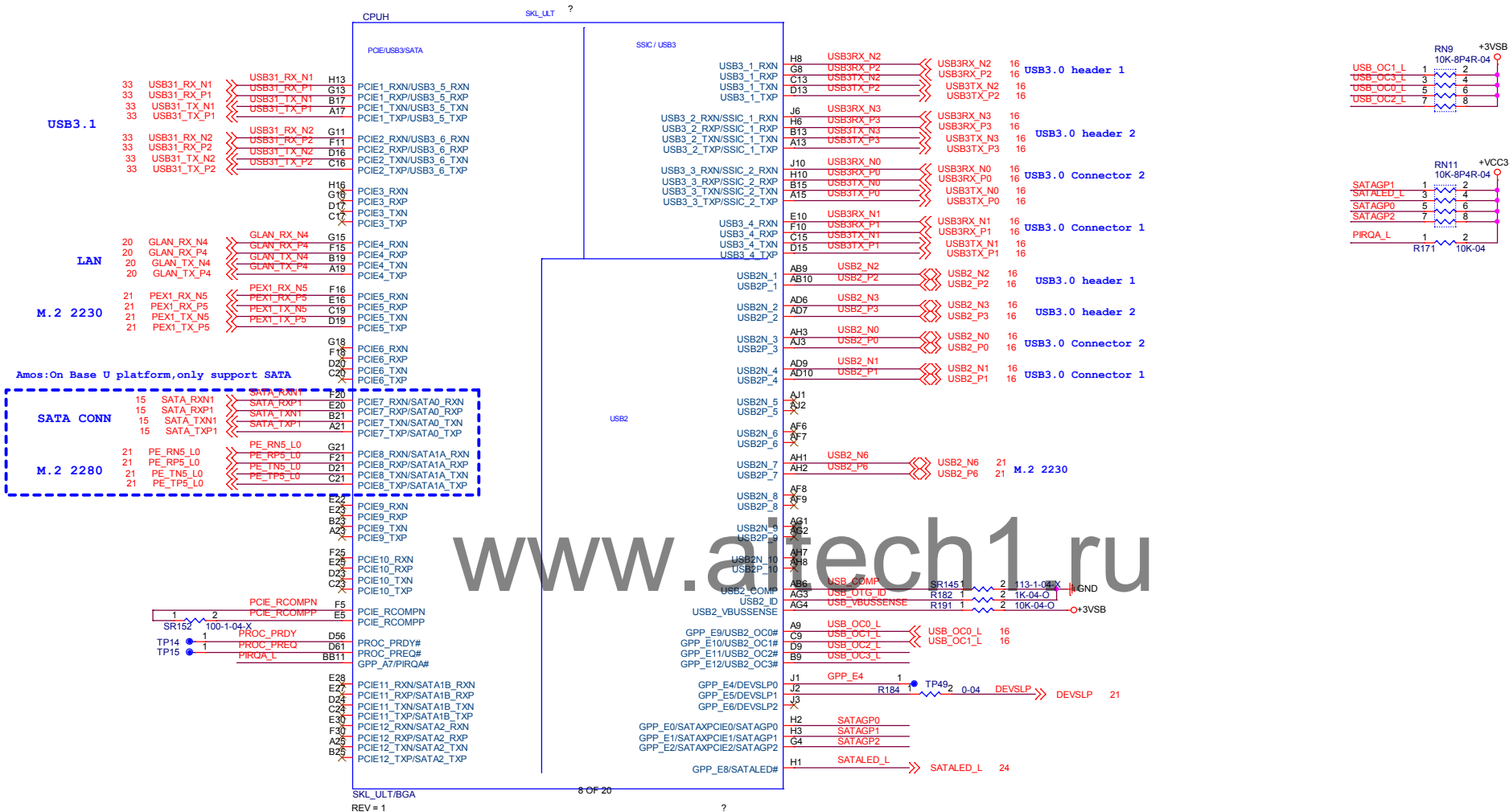
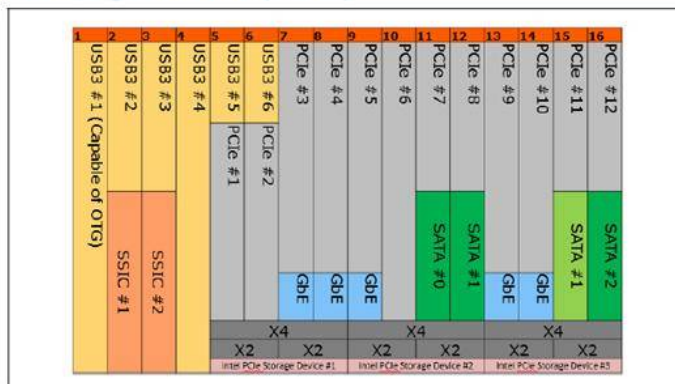
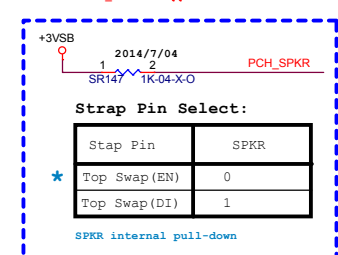
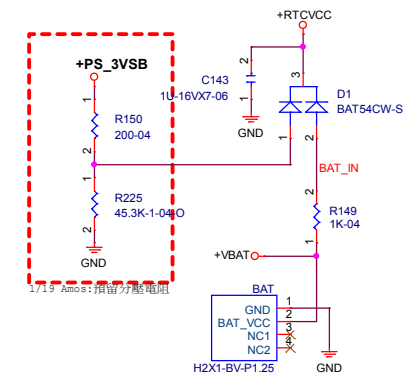
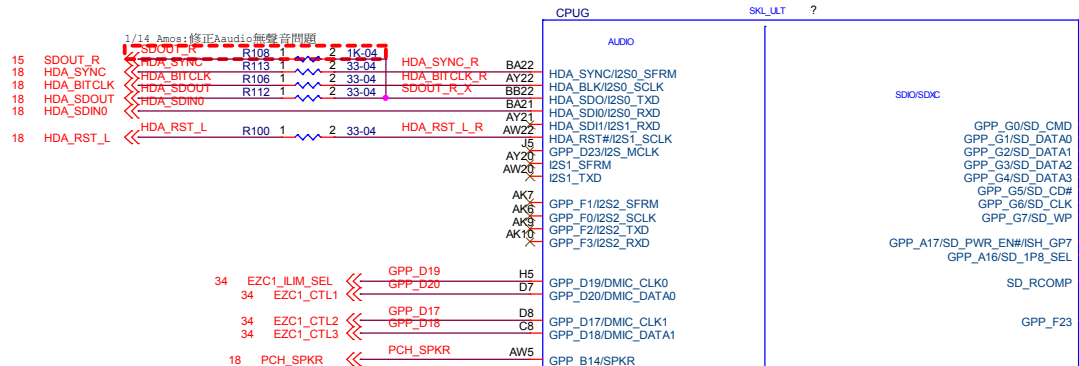


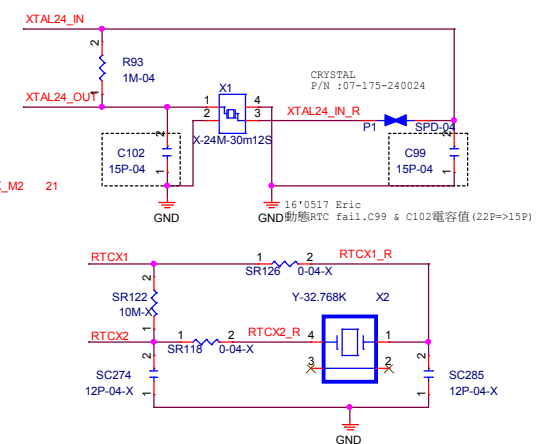
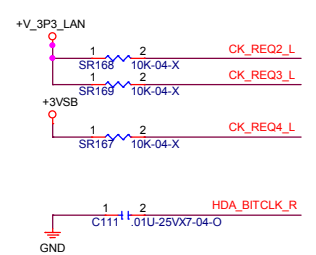
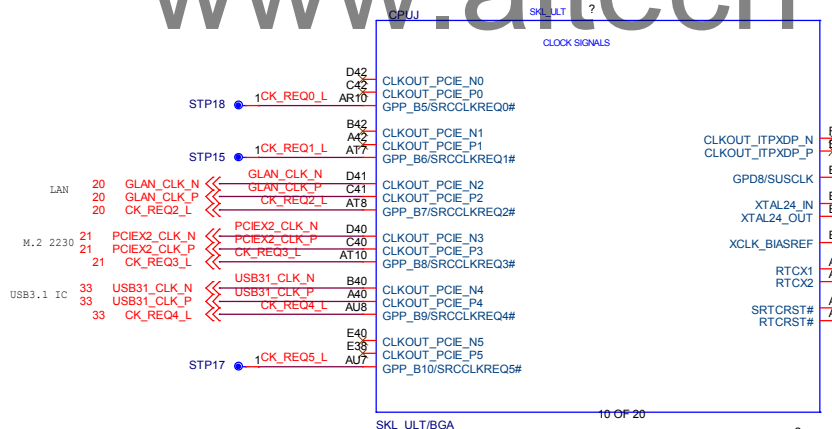
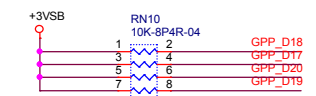
Figure 3-1. HSI0 Muxing on SKL PCH-LP (U Series)

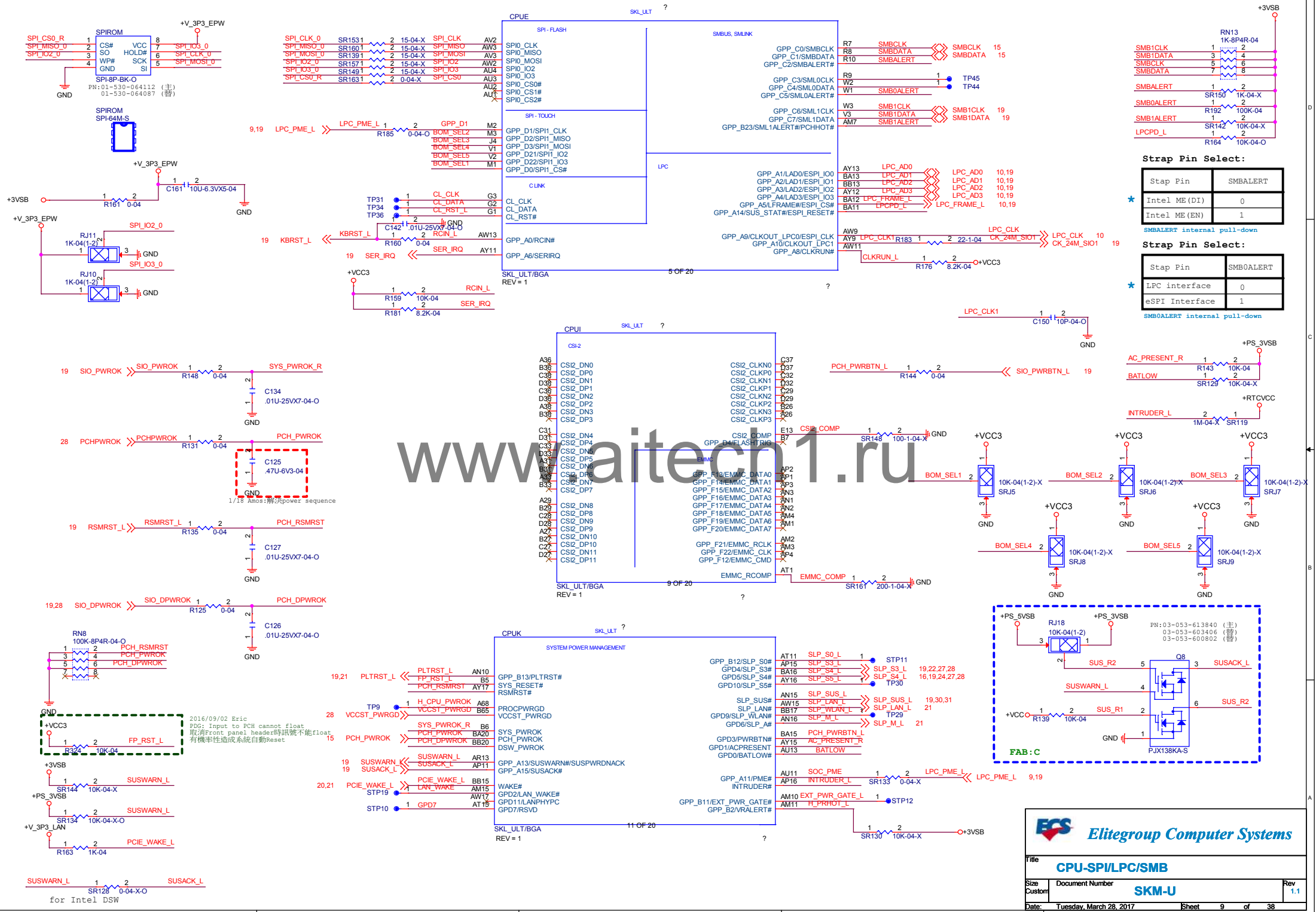






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Strap Pin Select:

Strap Pin	SMBALERT
Intel ME (DI)	0
Intel ME (EN)	1

Strap Pin Select:

Strap Pin	SMB0ALERT
LPC interface	0
eSPI Interface	1

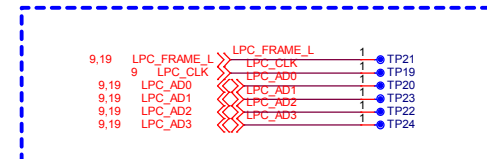
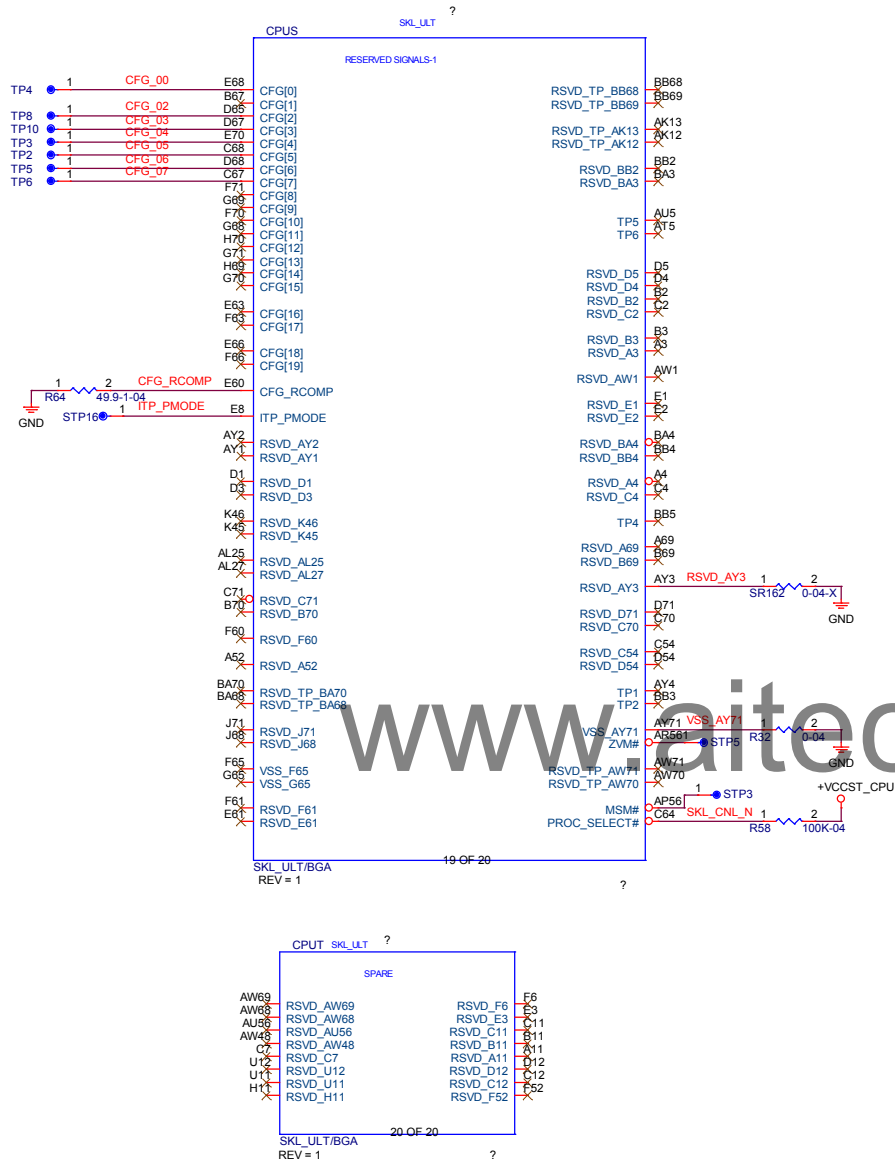
**CPU-SPI/LPC/SMB**

Document Number **SKM-U**

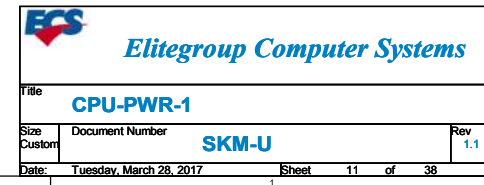
Date: Tuesday, March 28, 2017 Sheet 9 of 38

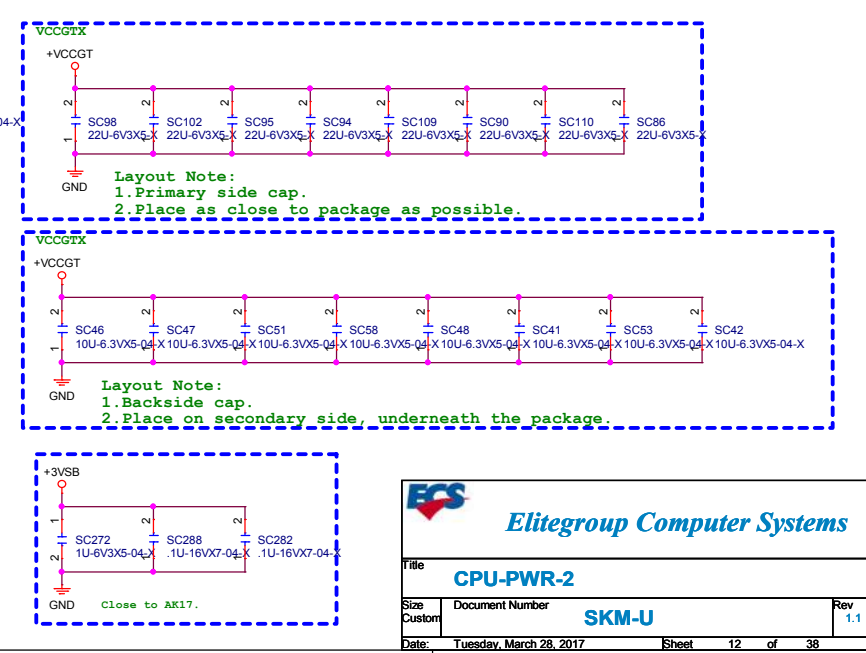
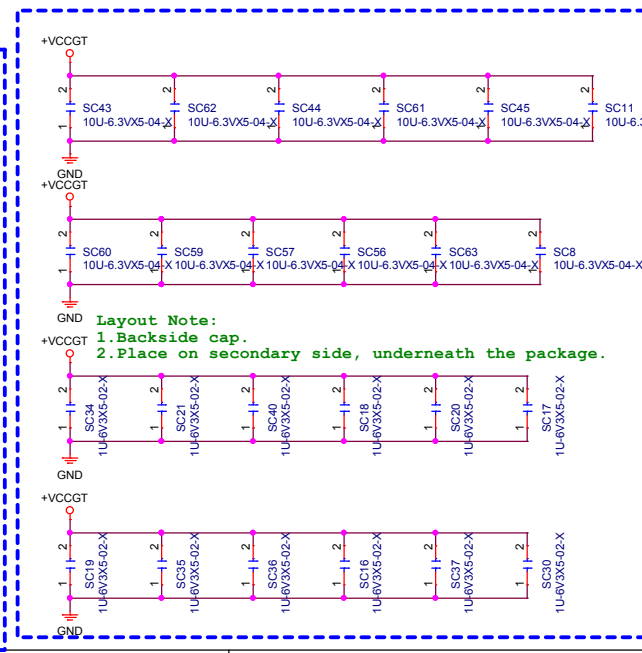
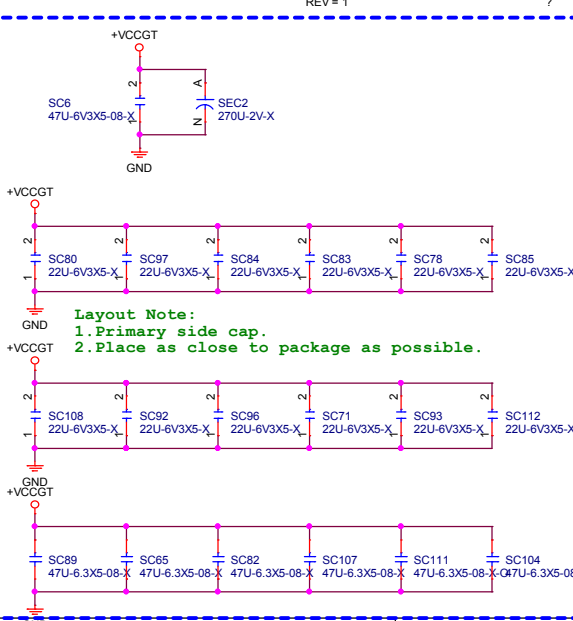
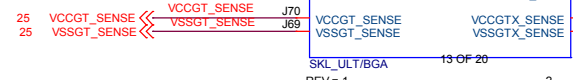
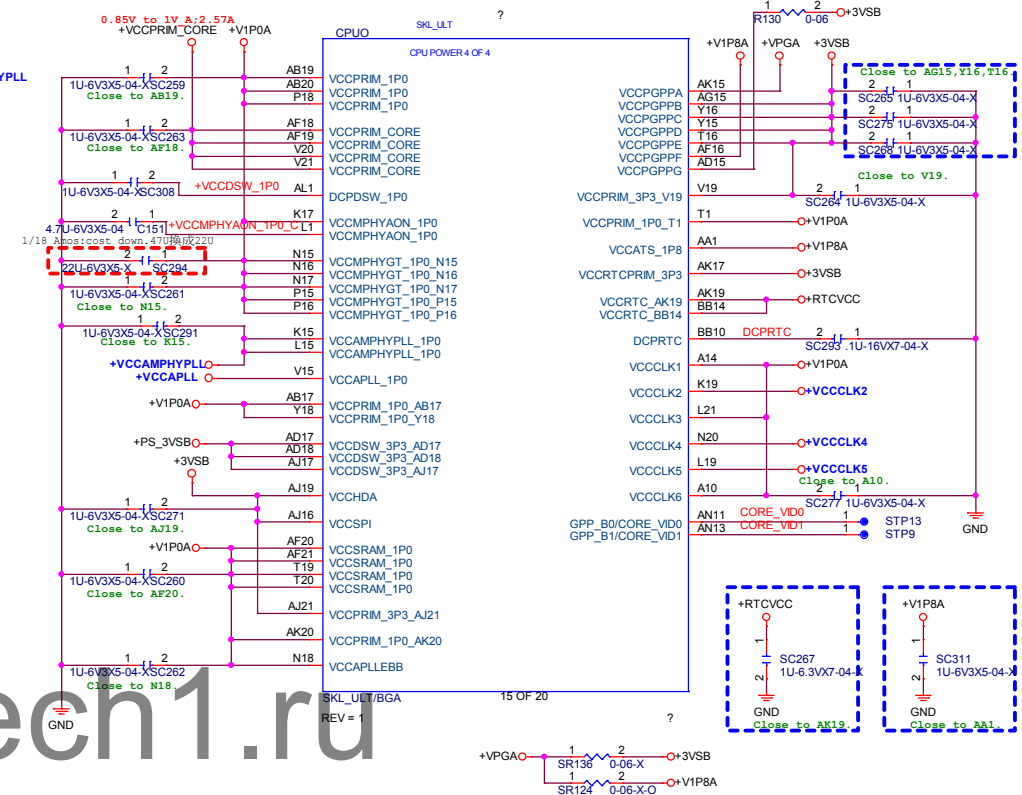
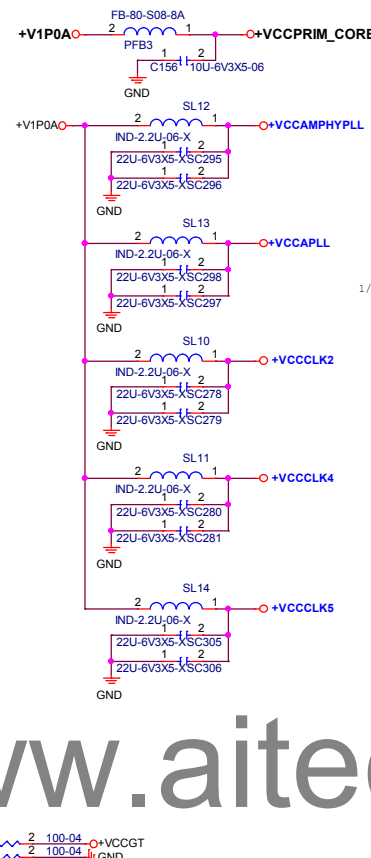
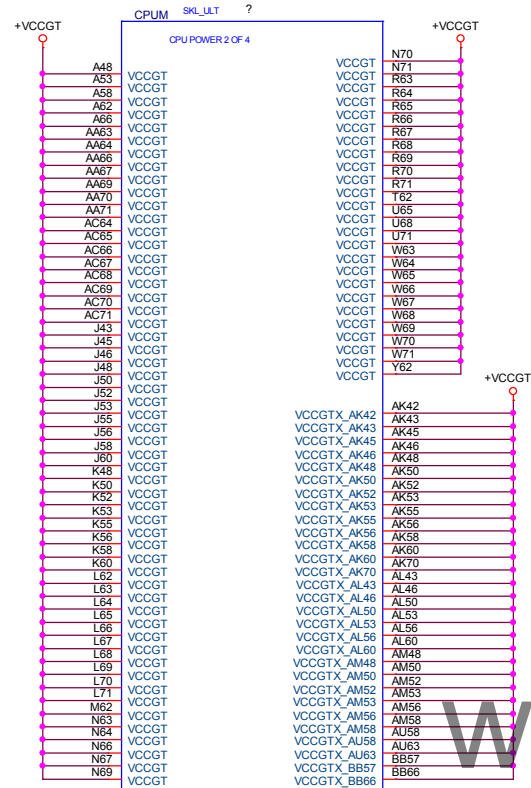
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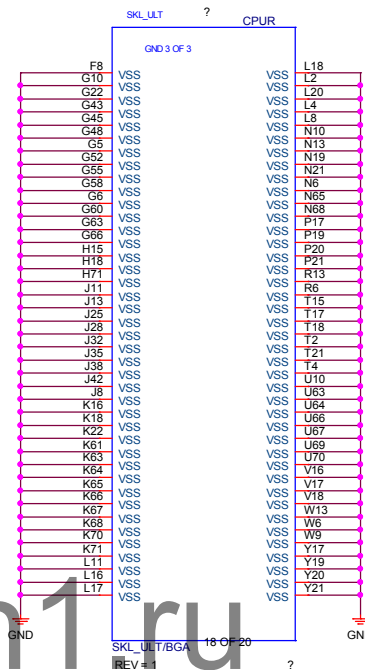
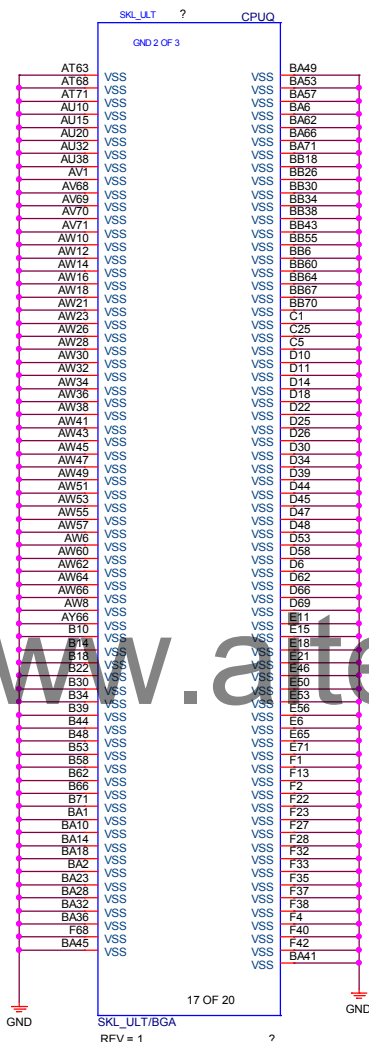
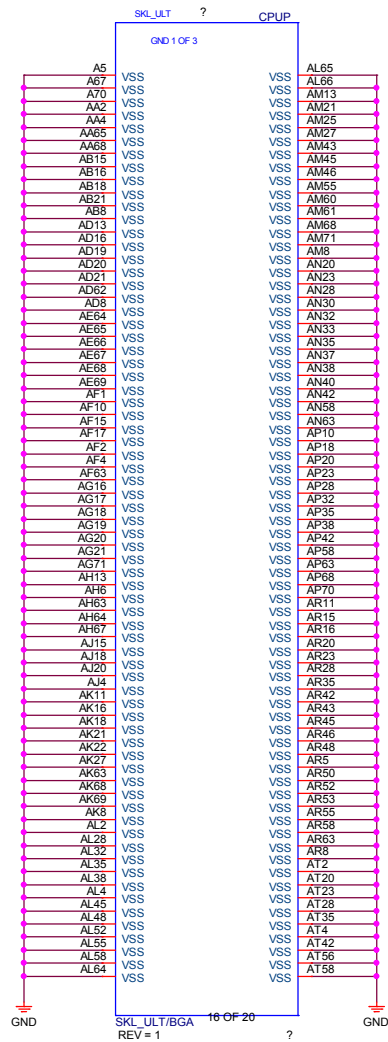




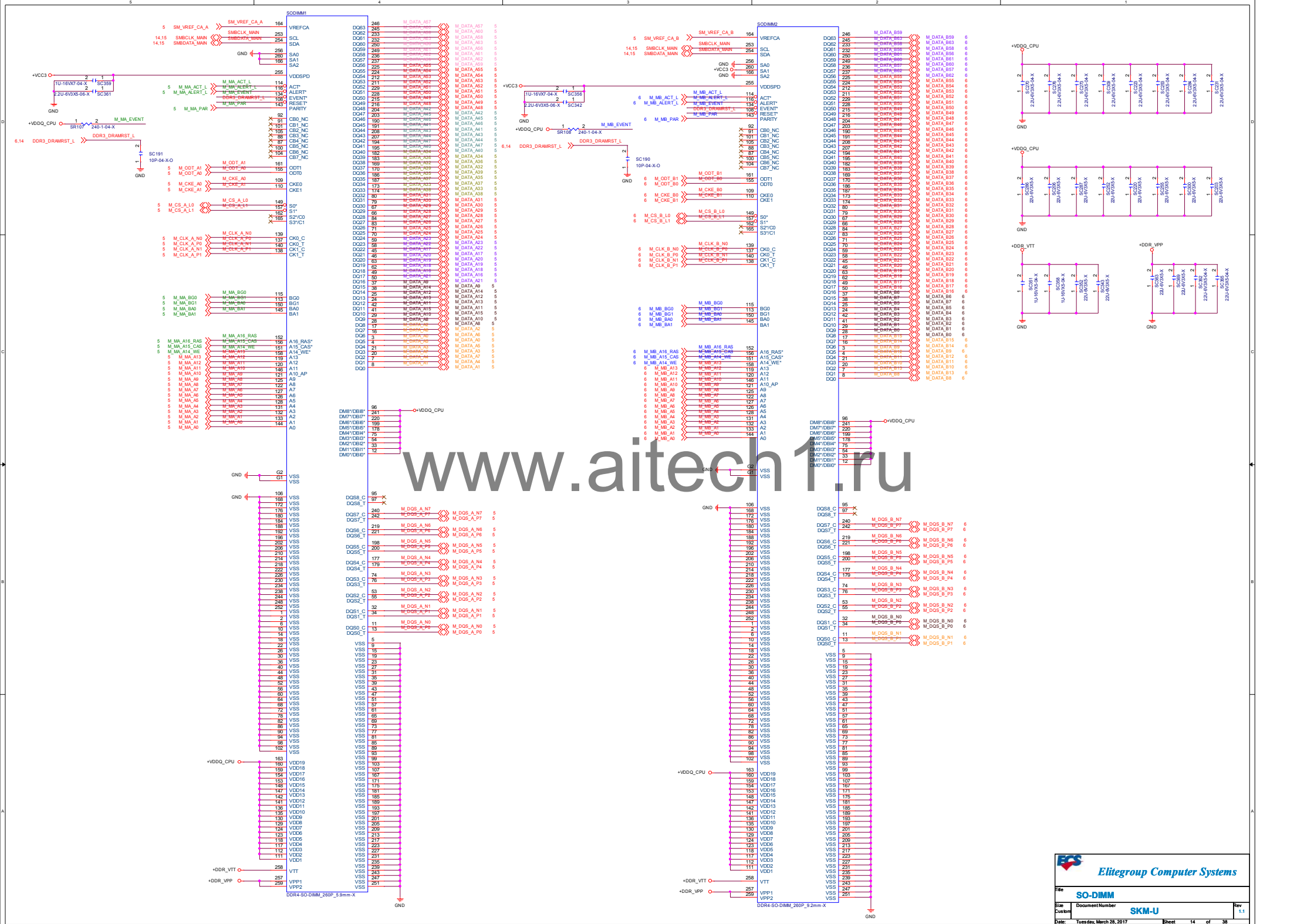
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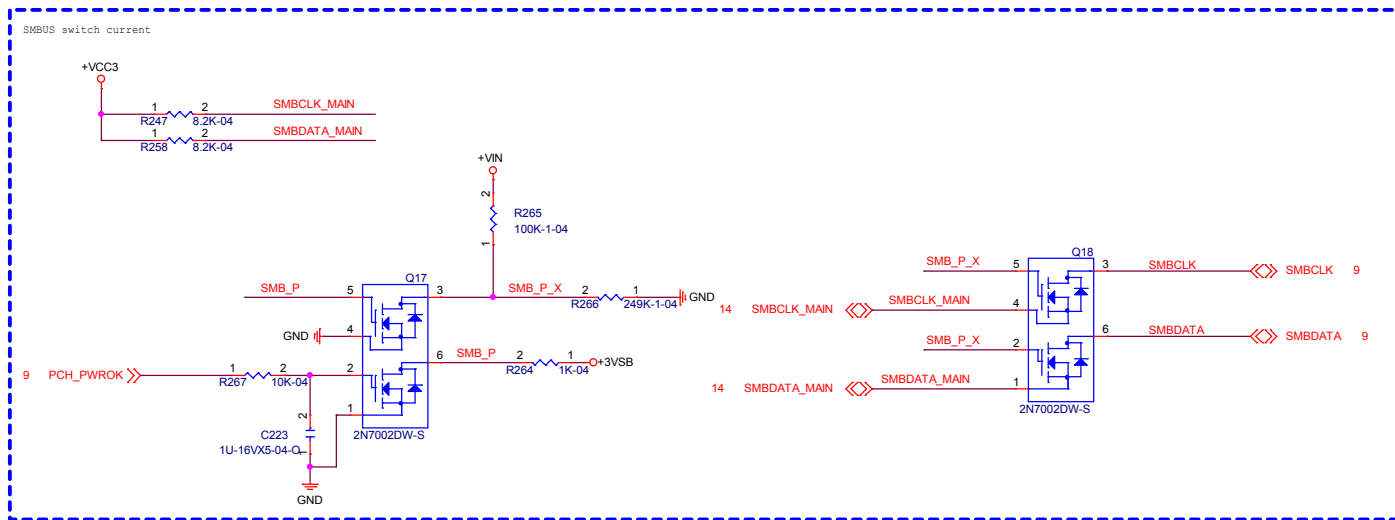




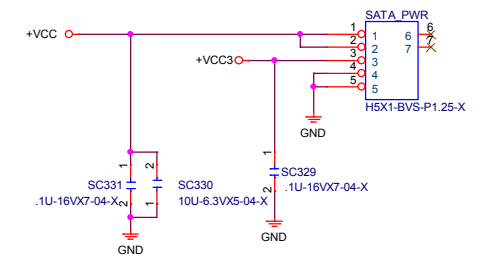
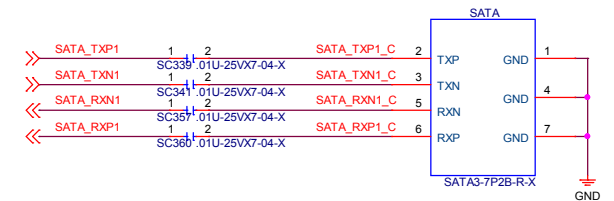


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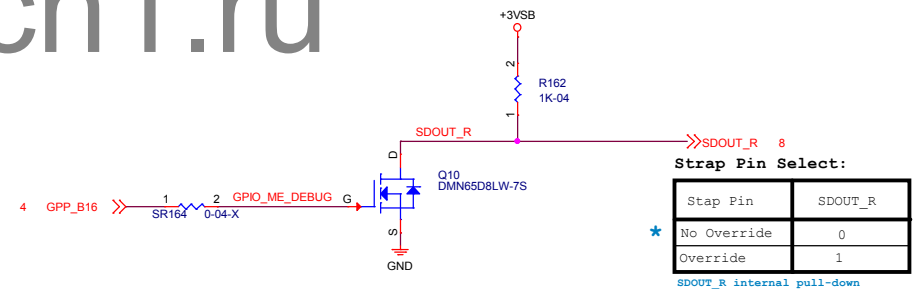
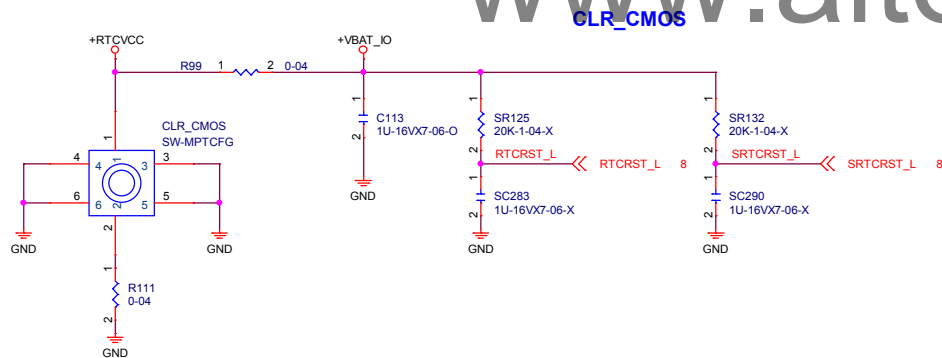




7 SATA\_TXP1  
7 SATA\_TXN1  
7 SATA\_RXN1  
7 SATA\_RXP1

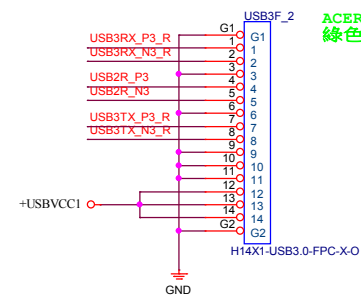
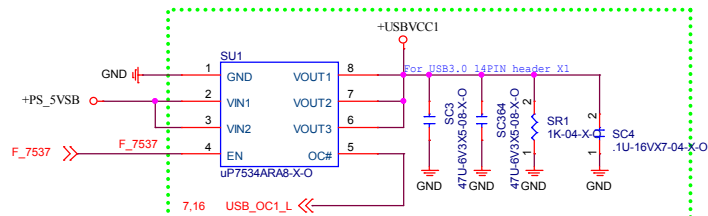
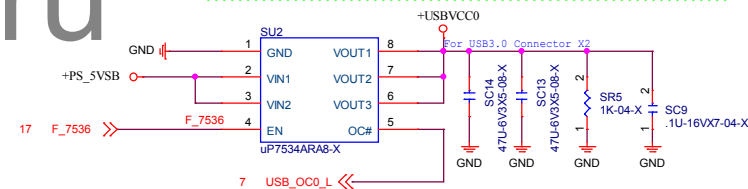
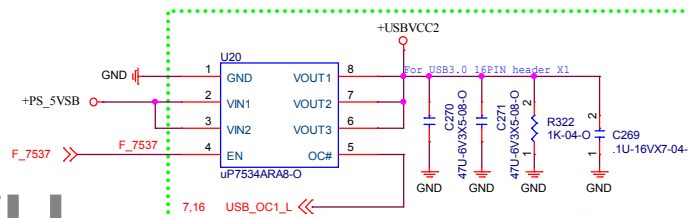
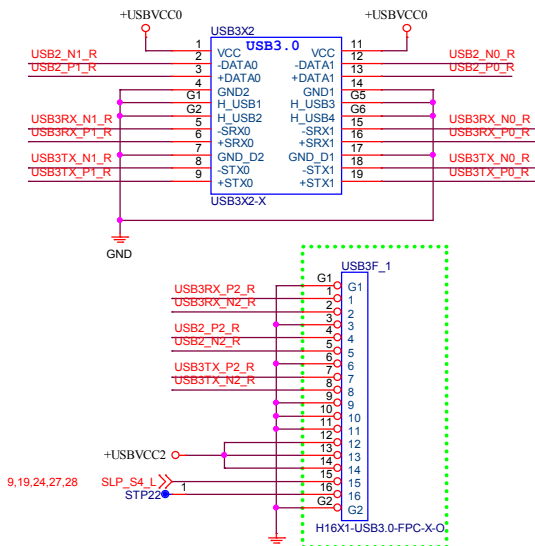
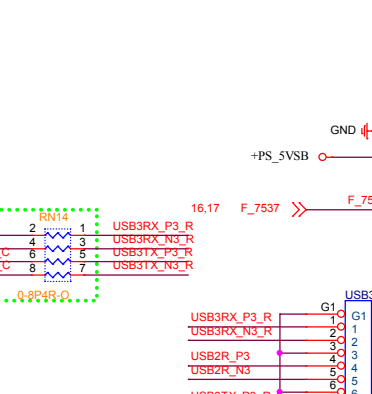
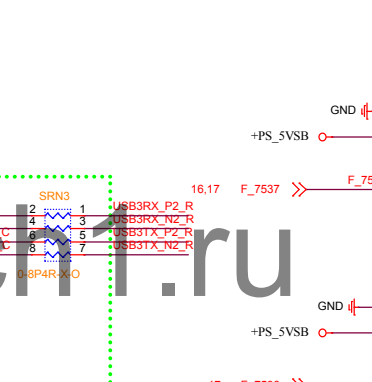
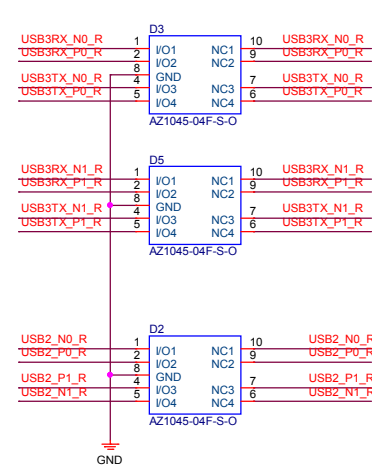
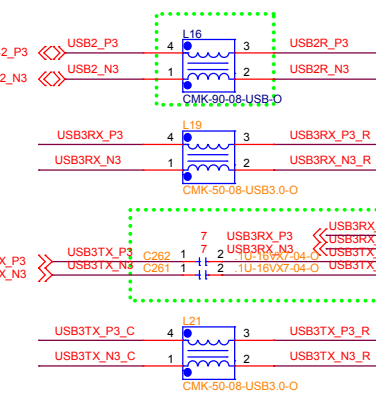
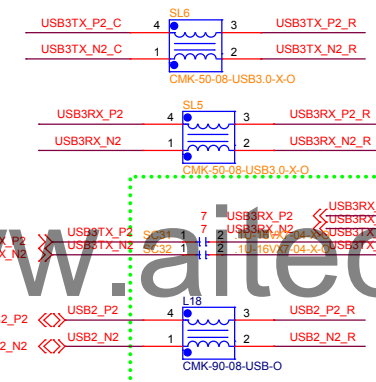
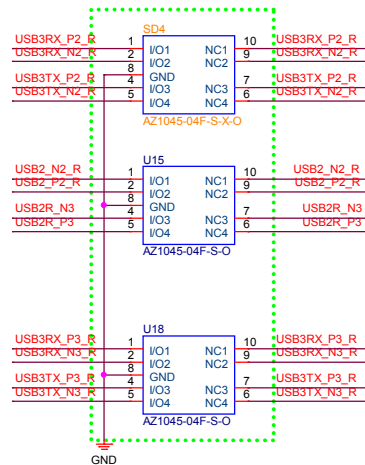
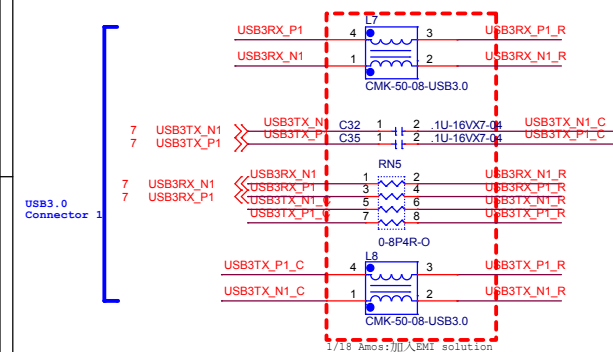
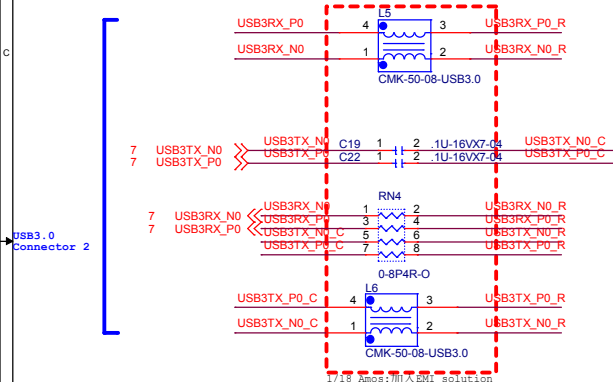
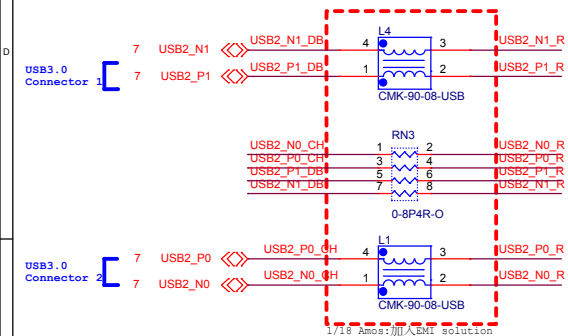


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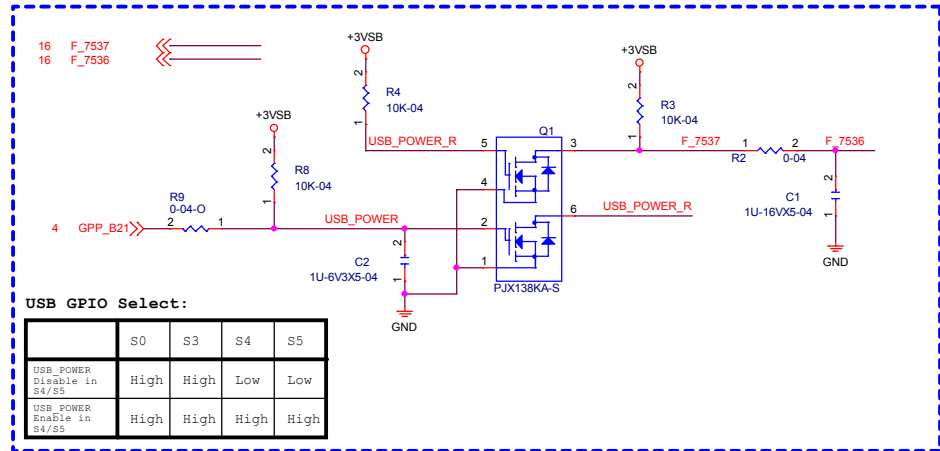
## USB3.0 Connector



20150805 Amos:Del USB Charging current

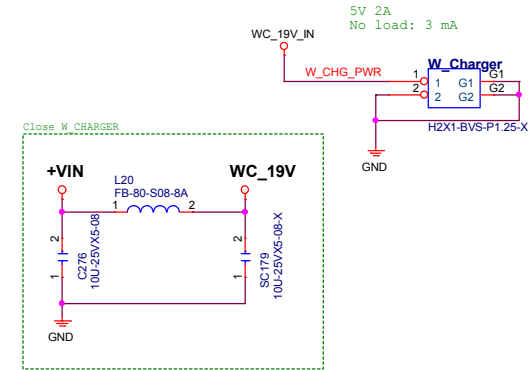
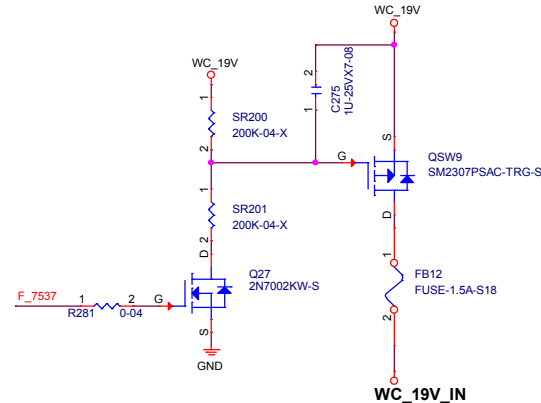
# USB 3.0 & 2.0 power Enable current

# Wireless charging header



USB GPIO Select:

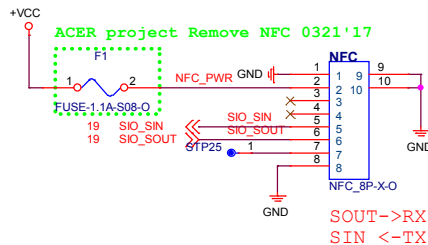
	S0	S3	S4	S5
USB_POWER Disable in S4/S5	High	High	Low	Low
USB_POWER Enable in S4/S5	High	High	High	High



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# LOGO LED header

# NFC header

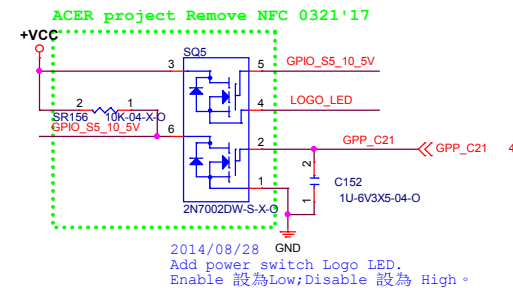
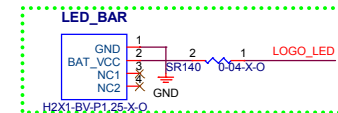


# NFC card PIN define

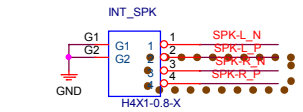
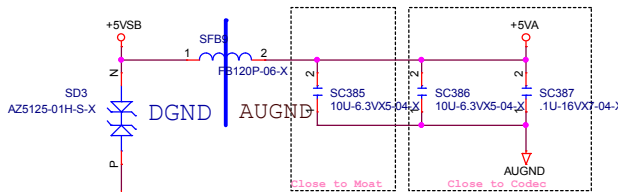
Cable PIN define:  
Card/Header  
1=>8 2=>7 3=>6  
4=>5 5=>4 6=>3  
7=>2 8=>1

# 2. Interface Connector

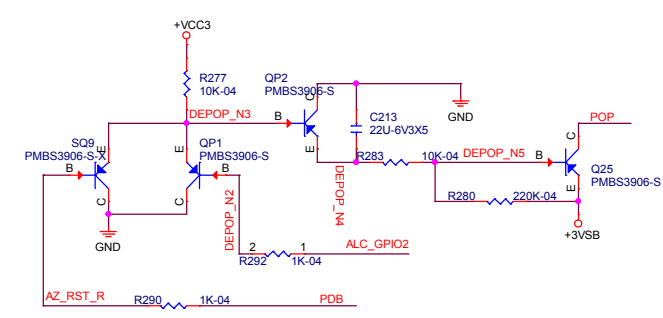
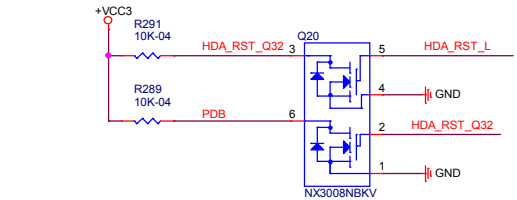
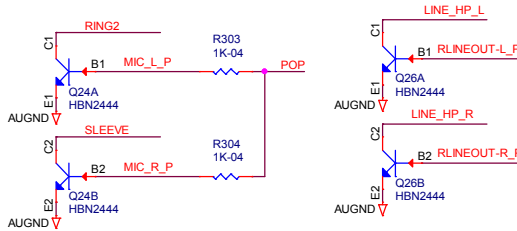
Pin Number	Definition	Description
1	GND	GND
2	RF	RF
3	TX	UART TX
4	Rx	UART RX
5	NC	NC
6	NC	NC
7	Vcc	Input VV
8	GND	GND



20150805 Amos:Del auxiliary Power connector

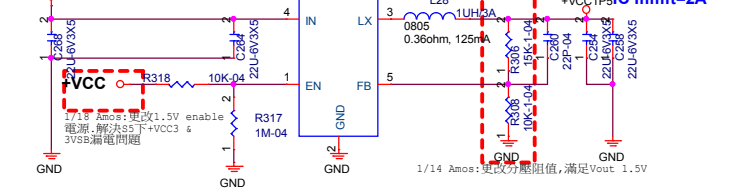


Speaker trace layout  
4 ohm : 40mil  
8 ohm : 20mil

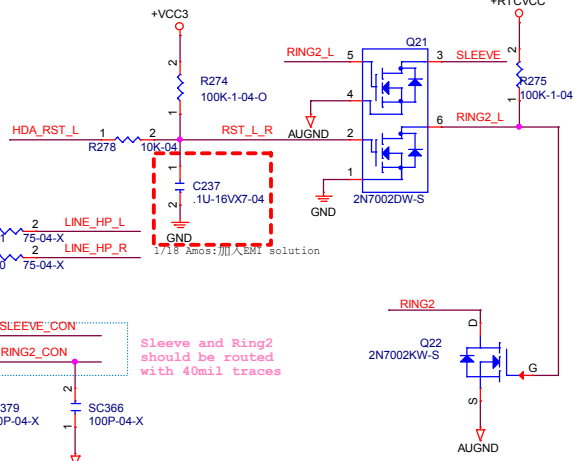
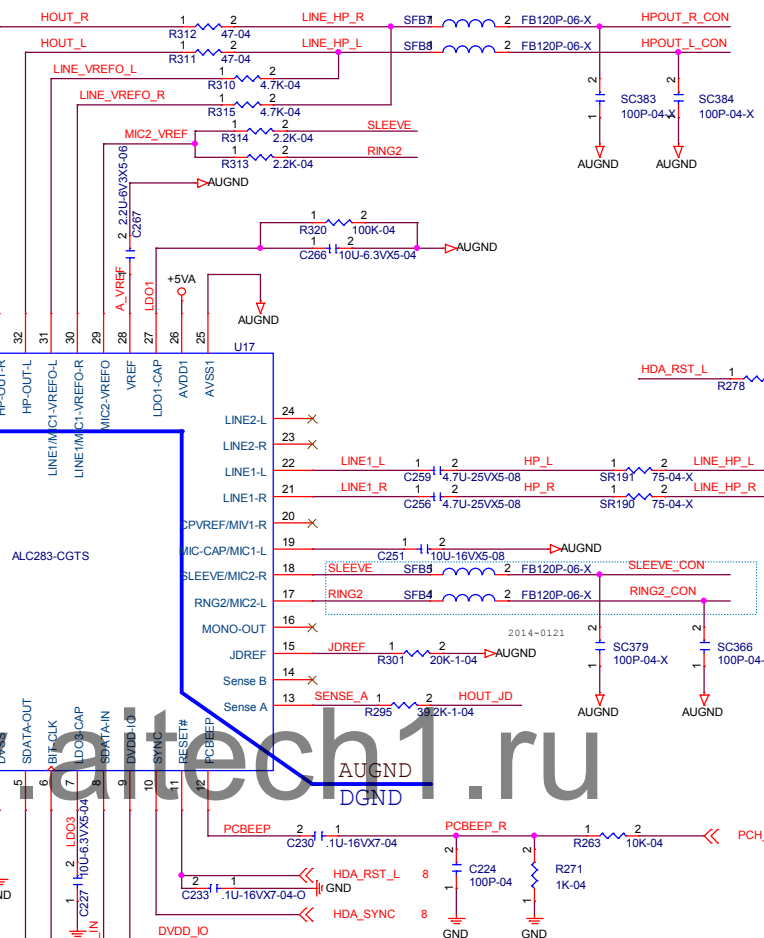


+VCC1P5

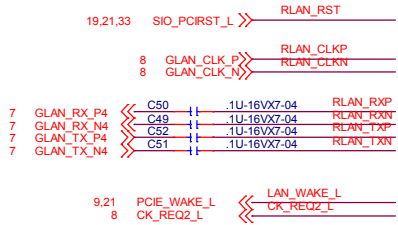
+PS\_3VSB



1/14 Amos:更改分壓阻值,滿足Vout 1.5V





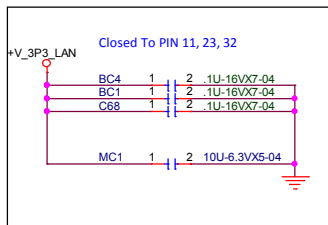
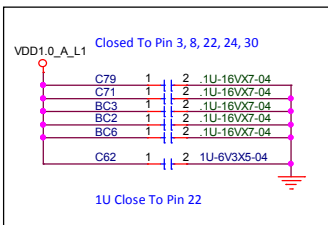
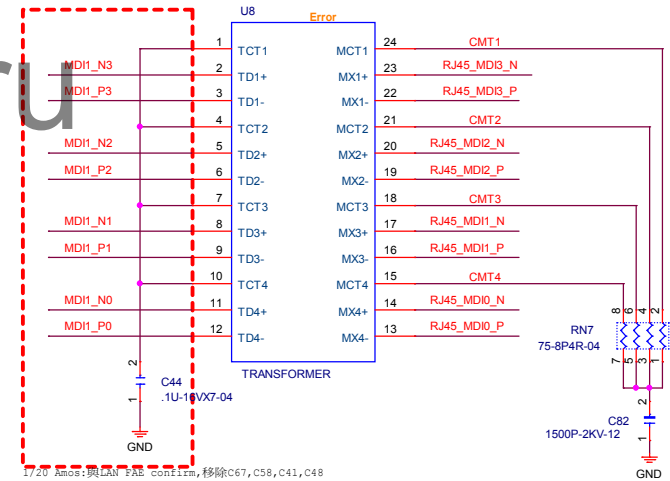
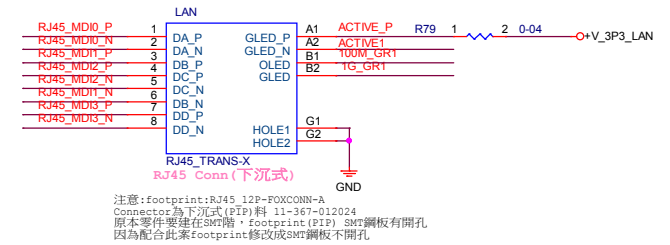
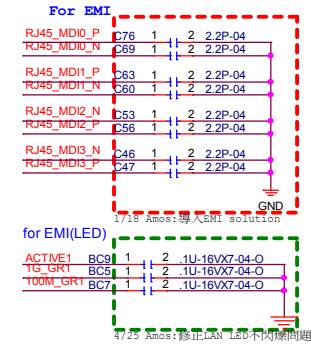
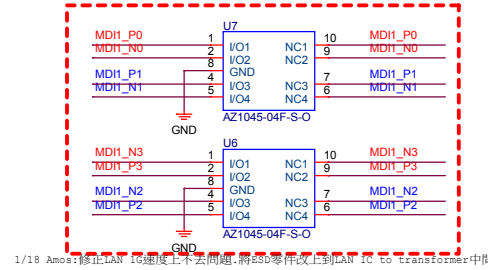
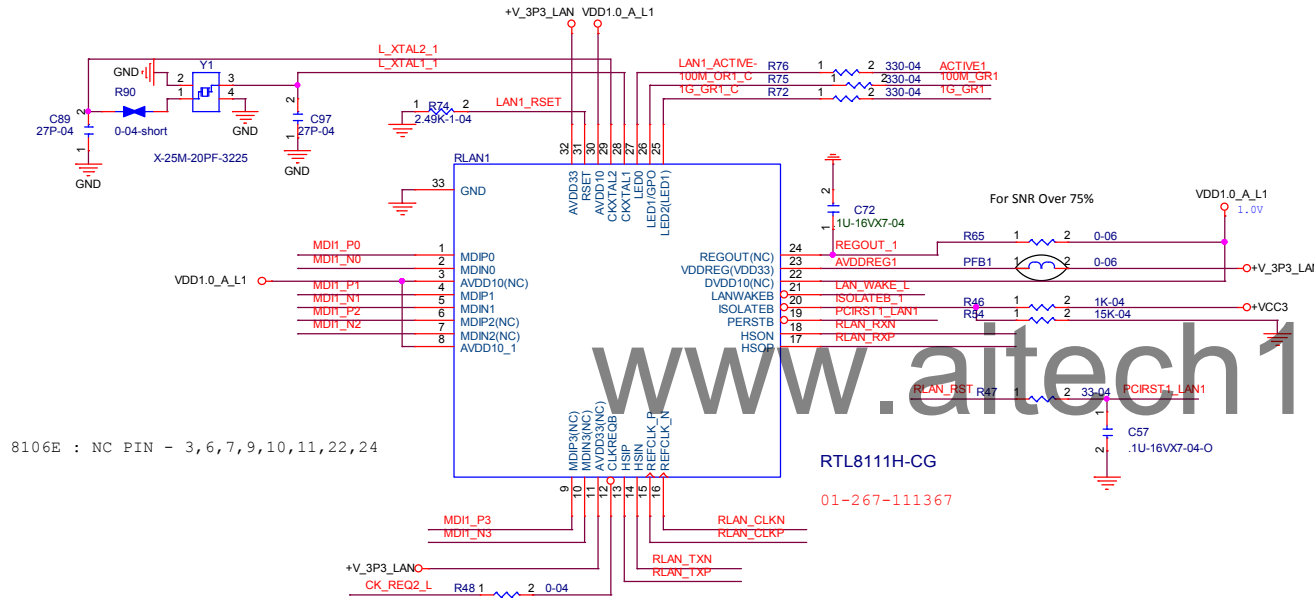


新手提醒:

LAN\_HSOP/N請接到SB的PCIE RX端

LAN\_HSIP/N請接到SB的PCIE TX端

LAN\_HSIP/N在SB的PCIE TX端要記得放AC coupling cap



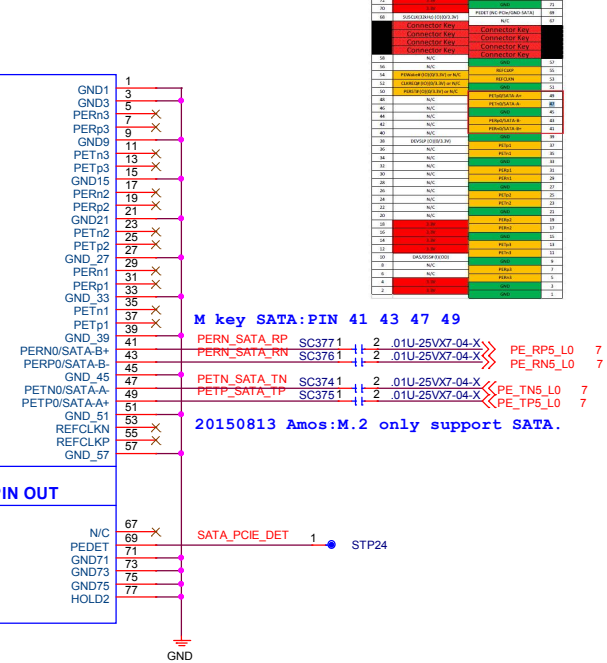
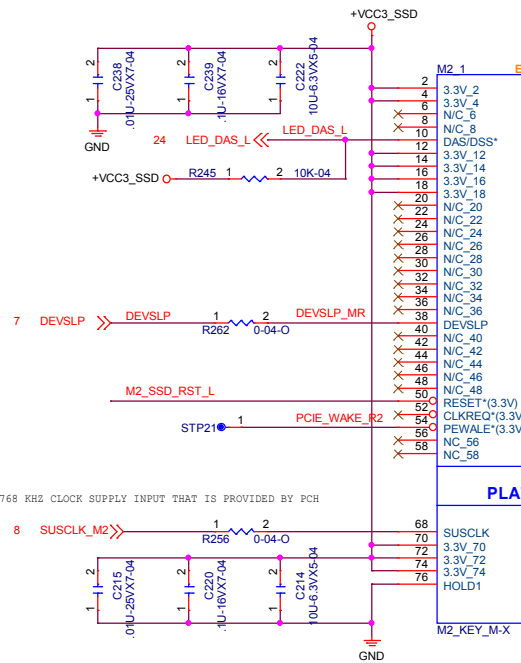
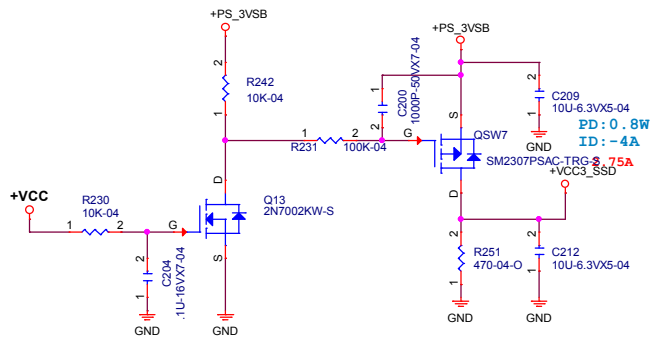
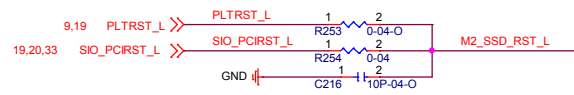
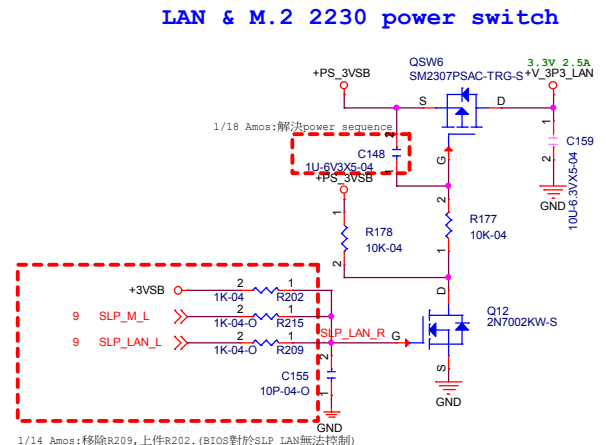
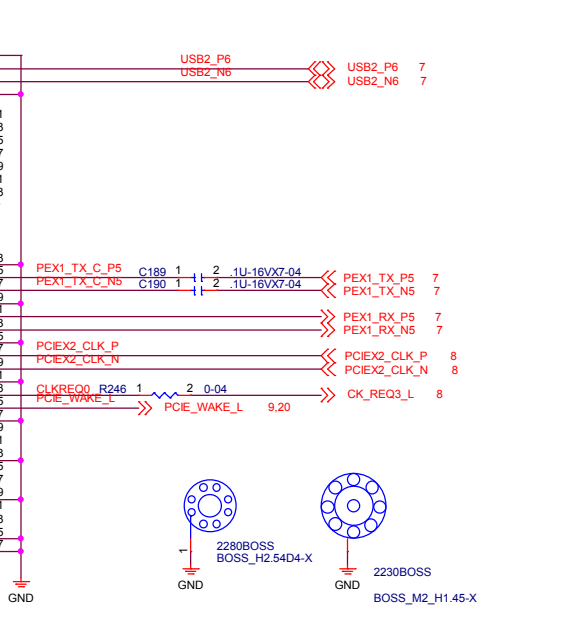
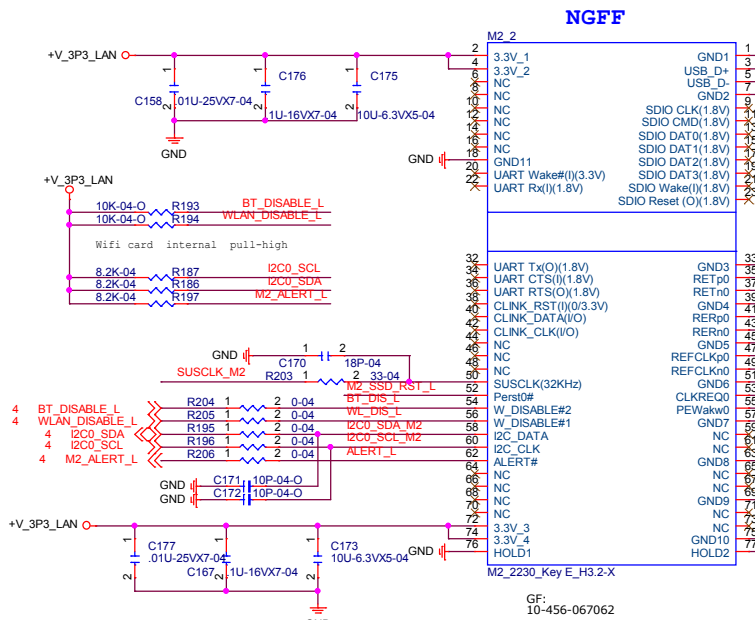


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Pin	Signal	Pin	Signal
1	NC	51	NC
2	NC	52	NC
3	NC	53	NC
4	NC	54	NC
5	NC	55	NC
6	NC	56	NC
7	NC	57	NC
8	NC	58	NC
9	NC	59	NC
10	NC	60	NC
11	NC	61	NC
12	NC	62	NC
13	NC	63	NC
14	NC	64	NC
15	NC	65	NC
16	NC	66	NC
17	NC	67	NC
18	NC	68	NC
19	NC	69	NC
20	NC	70	NC
21	NC	71	NC
22	NC	72	NC
23	NC	73	NC
24	NC	74	NC
25	NC	75	NC
26	NC	76	NC
27	NC	77	NC
28	NC	78	NC
29	NC	79	NC
30	NC	80	NC
31	NC	81	NC
32	NC	82	NC
33	NC	83	NC
34	NC	84	NC
35	NC	85	NC
36	NC	86	NC
37	NC	87	NC
38	NC	88	NC
39	NC	89	NC
40	NC	90	NC
41	NC	91	NC
42	NC	92	NC
43	NC	93	NC
44	NC	94	NC
45	NC	95	NC
46	NC	96	NC
47	NC	97	NC
48	NC	98	NC
49	NC	99	NC
50	NC	100	NC

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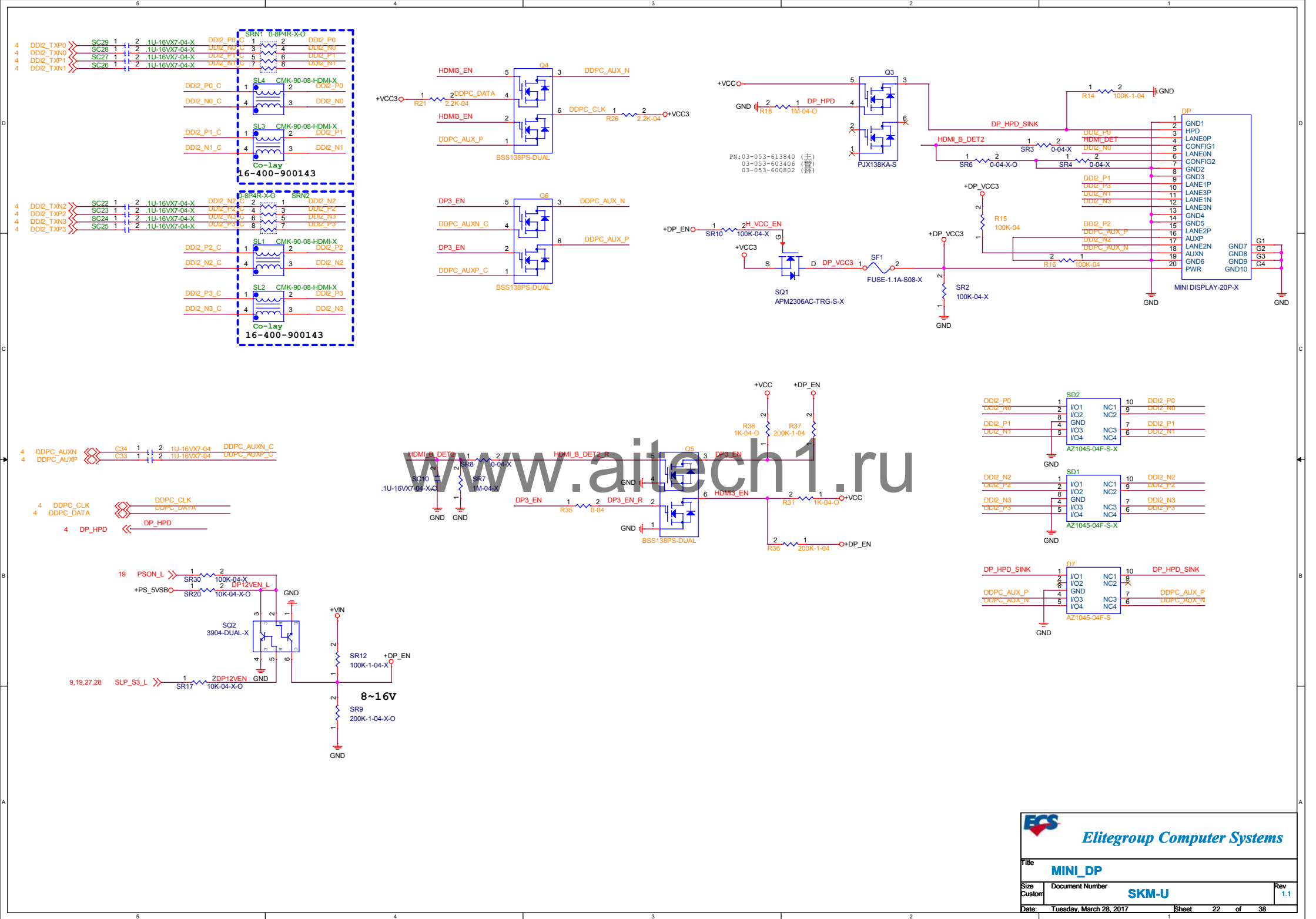
**M.2 2280/2230**

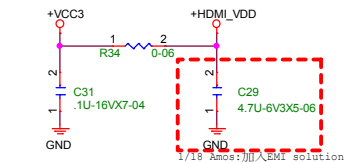
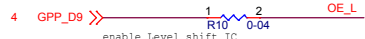
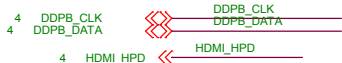
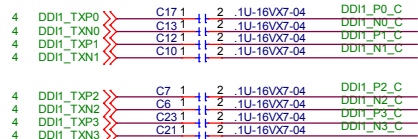
Document Number: **SKM-U**

Date: Tuesday, March 28, 2017

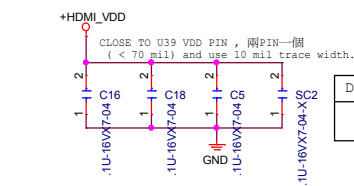
Sheet 21 of 38



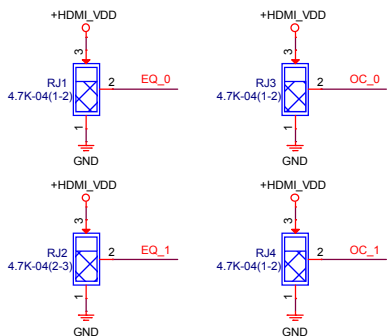




CLOSE TO POWER PLANE TO 1442K



DDC_EN	Passgate
3.3V	Enable
	Disable

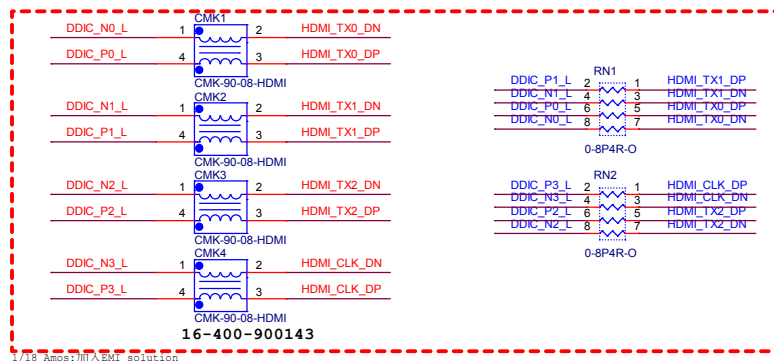


## TMDS Input Signal Equalization

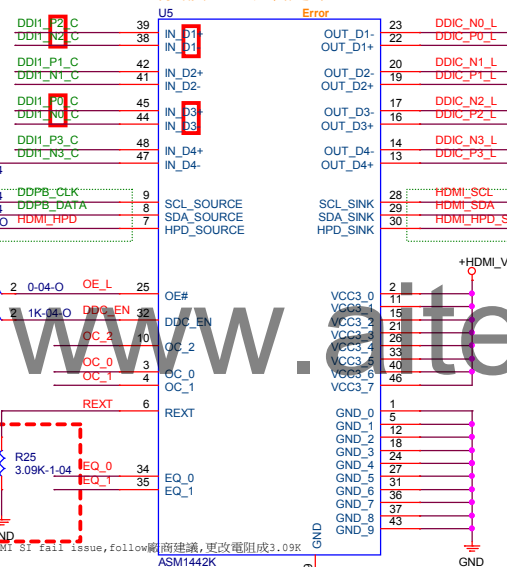
EQ_1	EQ_0	Equalization	Note
0	0	6dB	
0	1	3dB	
1	0	1dB	Default
1	1	0dB	

## TMDS Output Signal Integrity

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note
0	0	0	450	0	0	
0	0	1	420	0	-3dB	Shortest trace
0	1	0	450	0	-3dB	Shortest trace
0	1	1	460	0	-4dB	
1	0	0	340	0	0	
1	0	1	400	2dB	0	Longest trace
1	1	0	400	2dB	0	Longest trace
1	1	1	420	0	0	

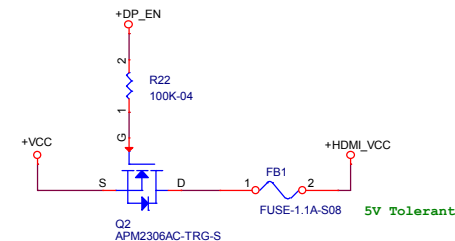
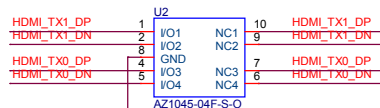
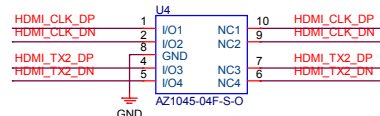


IC 跟connector同面or反面  
 可交換lane以利走線



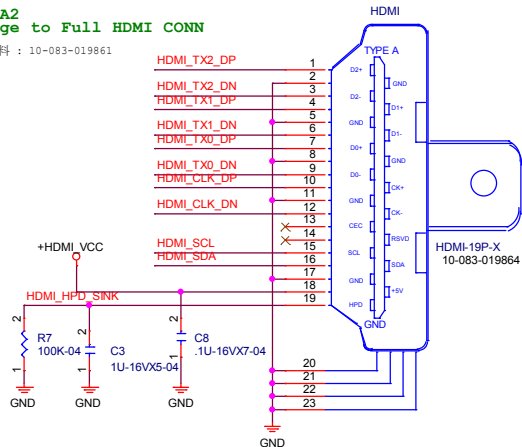
HD_HPD	Status
Hi	Plugged
Lo	Unplugged

HD\_HPD: internal 100K pull low

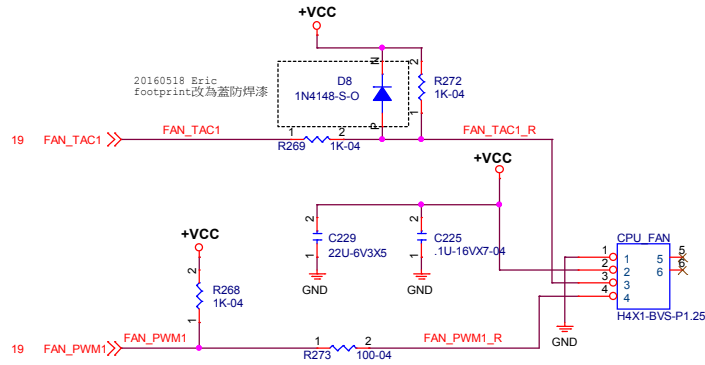


## FAB:A2 Change to Full HDMI CONN

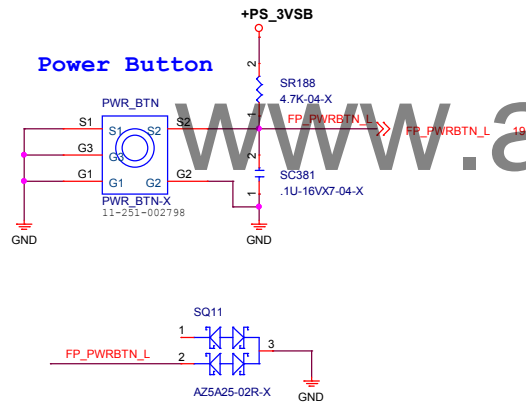
HDMI 替料: 10-083-019861



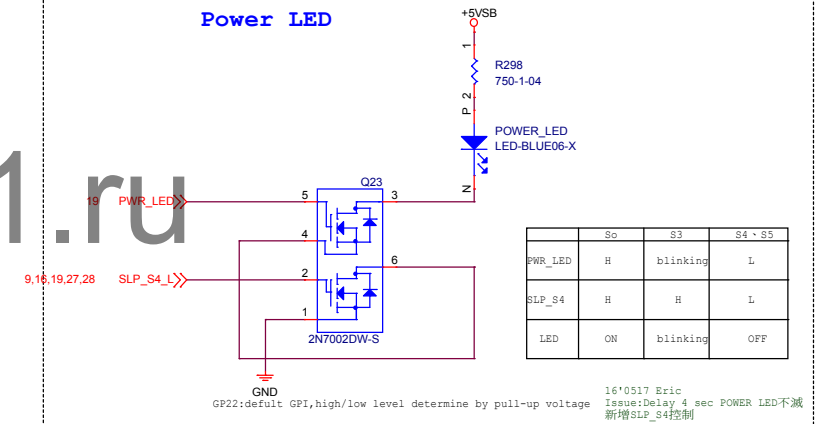
## FAN CONTROL header



## Power Button



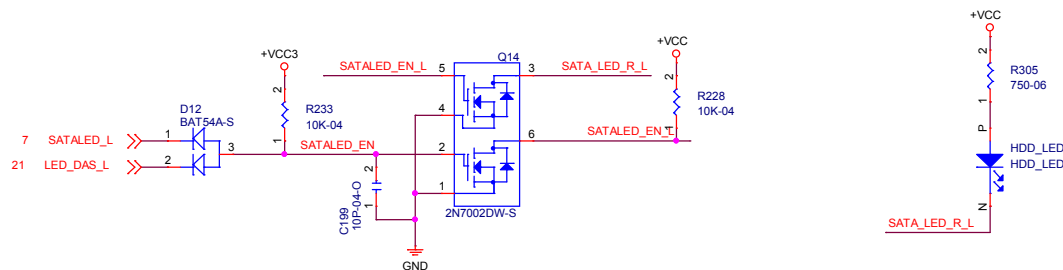
## Power LED



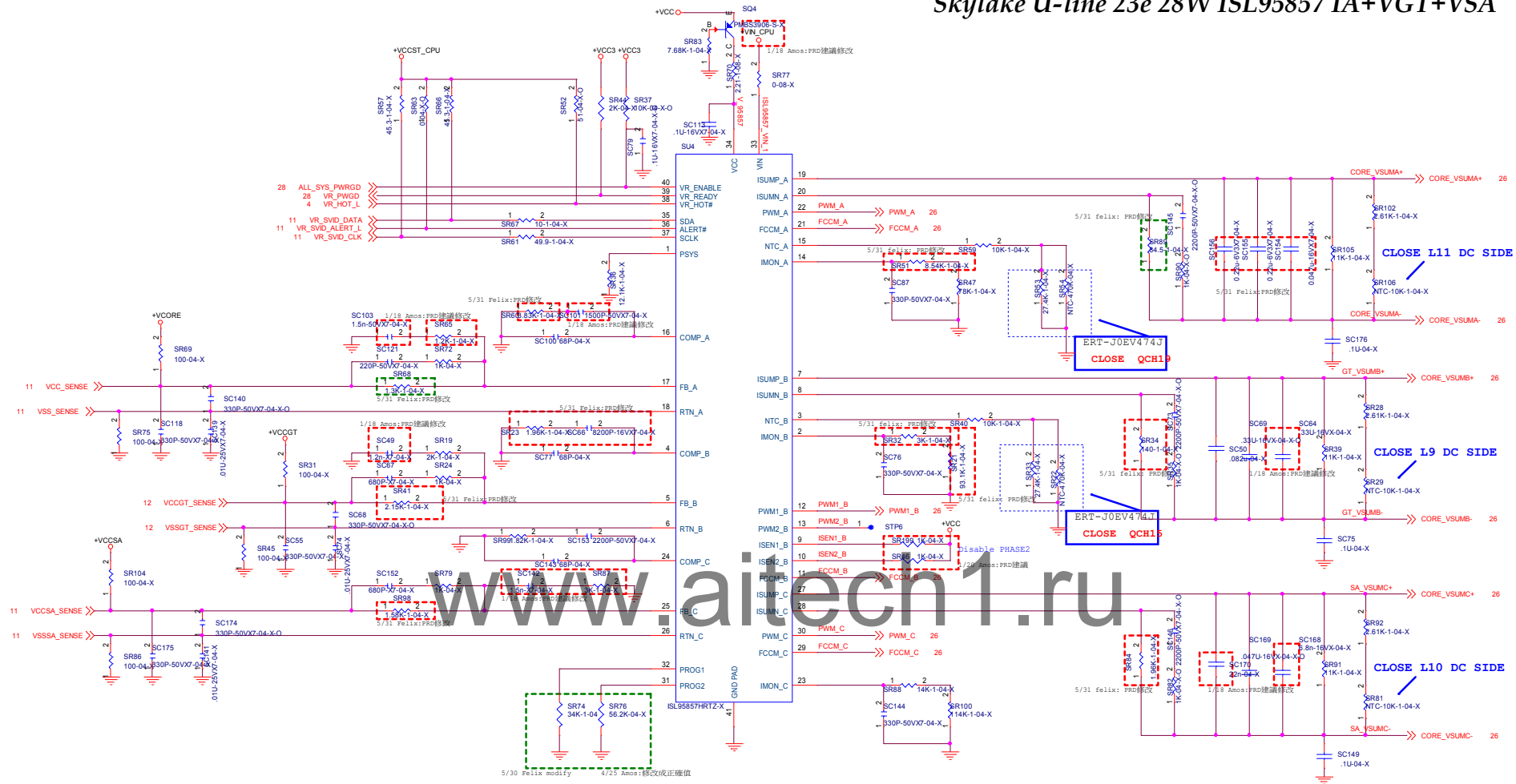
## 6. List of GPIO Pins

Table 6-1. GPIO Alternate Function

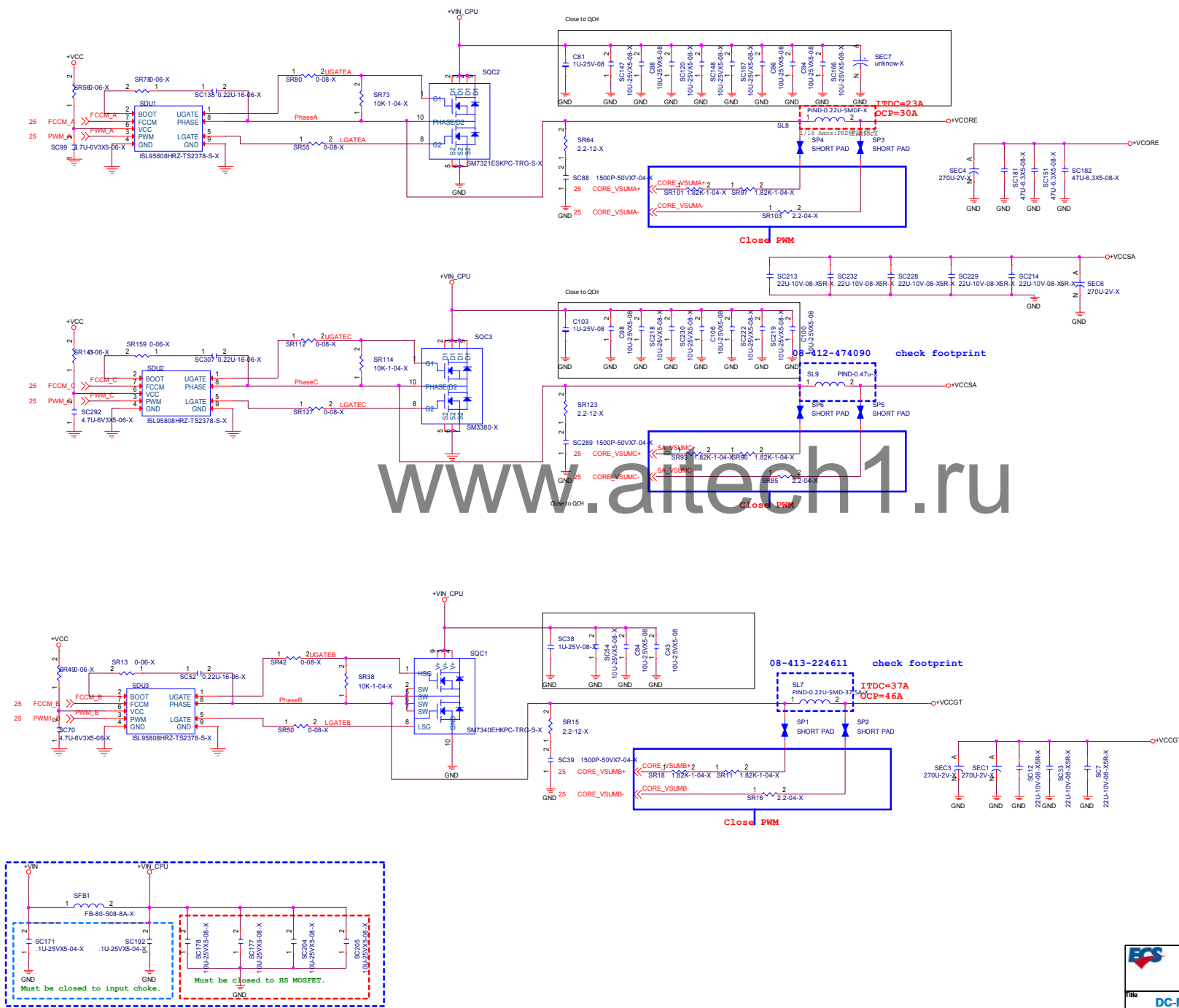
Group	Bit	Power By	Pin Loc.	1 <sup>st</sup> Func	Condition	2 <sup>nd</sup> Func	Condition	3 <sup>rd</sup> Func	Condition	4 <sup>th</sup> Func	Condition	Output Driving (mA)	Note
GPIO 1k	0	3VSB	40	PC10D170P (D10C10)		GPIO10A (D1)	250-0-0	GPIO10B (D10C10)	250-0-1			8mA	
	2	3VSB	11	PC10D170P (D10C10)		GPIO11A (D10C10)	250-0-1					8mA	
GP IO2k	0	3VSB	8	GPIO2A (D10C10)	250-0-1							8mA	
	3	3VSB	8	GPIO2B (D10C10)	250-0-1							8mA	



# Skylake U-line 23e 28W ISL95857 IA+VGT+VSA

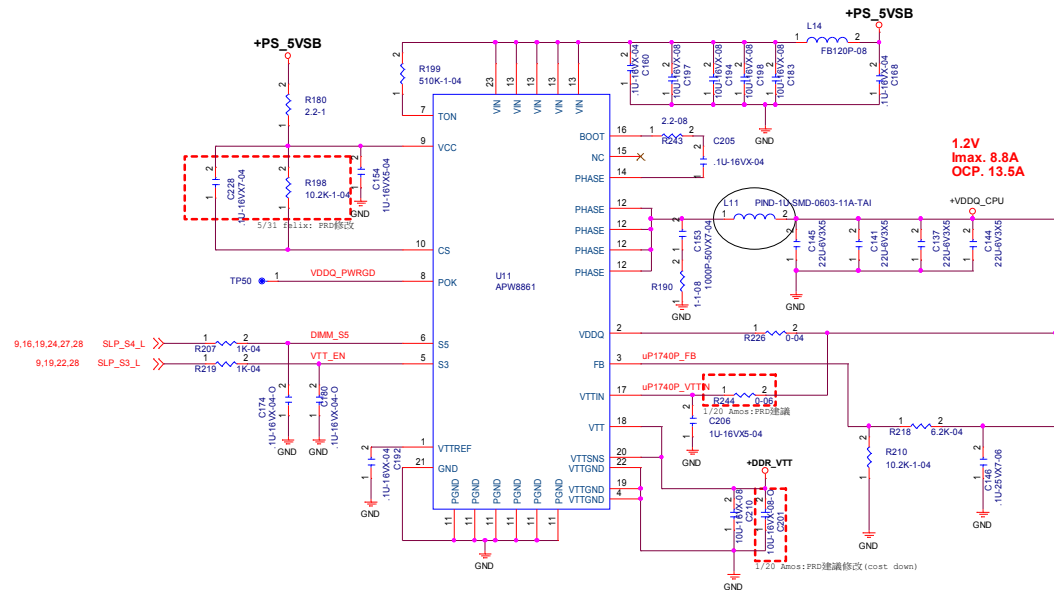


# IMVP8 ISL95853 VCCGT Schematic

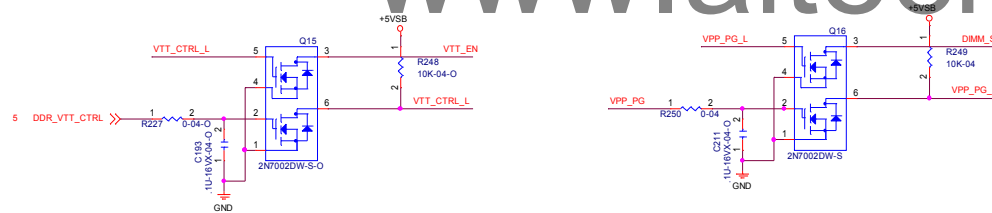


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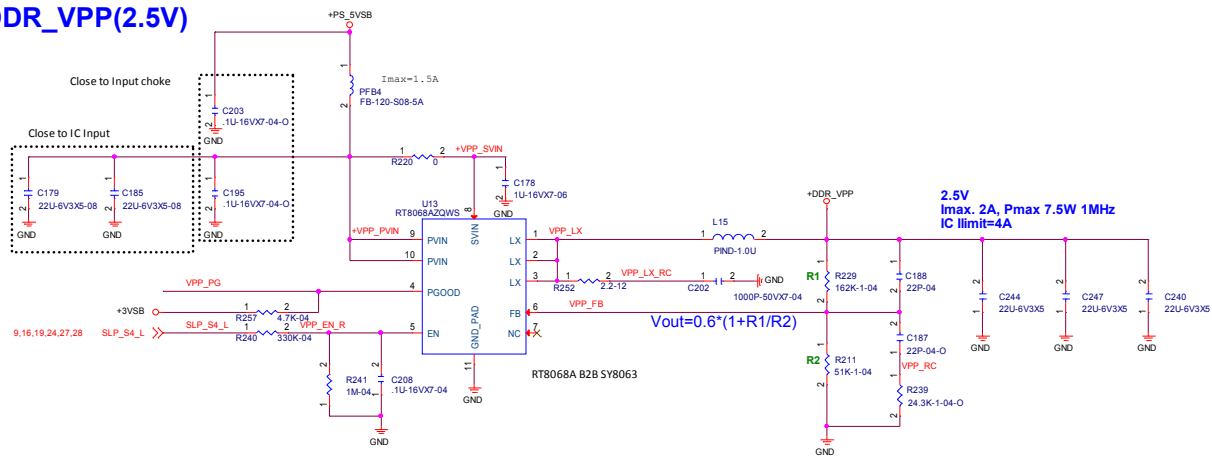
**+VDDQ(1.2V)**



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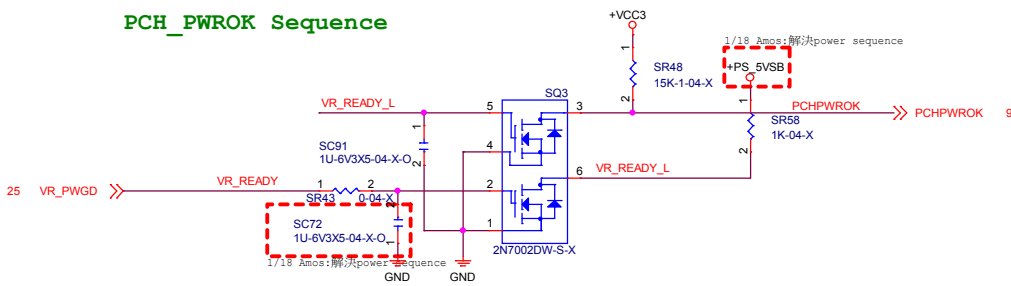


**+DDR\_VPP(2.5V)**

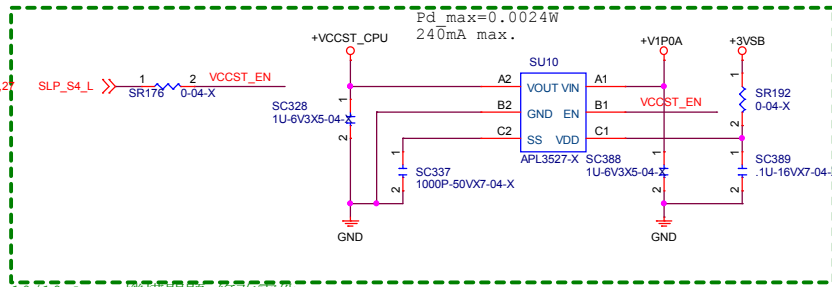
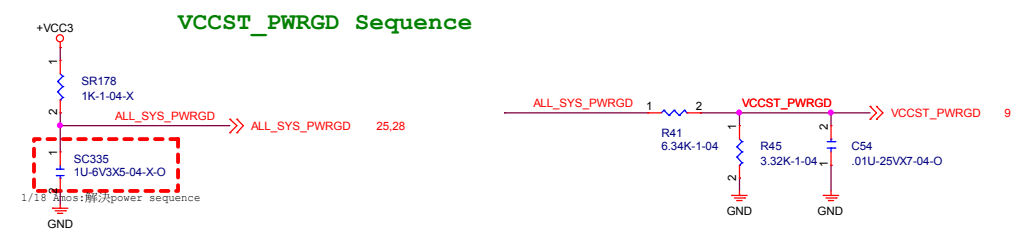




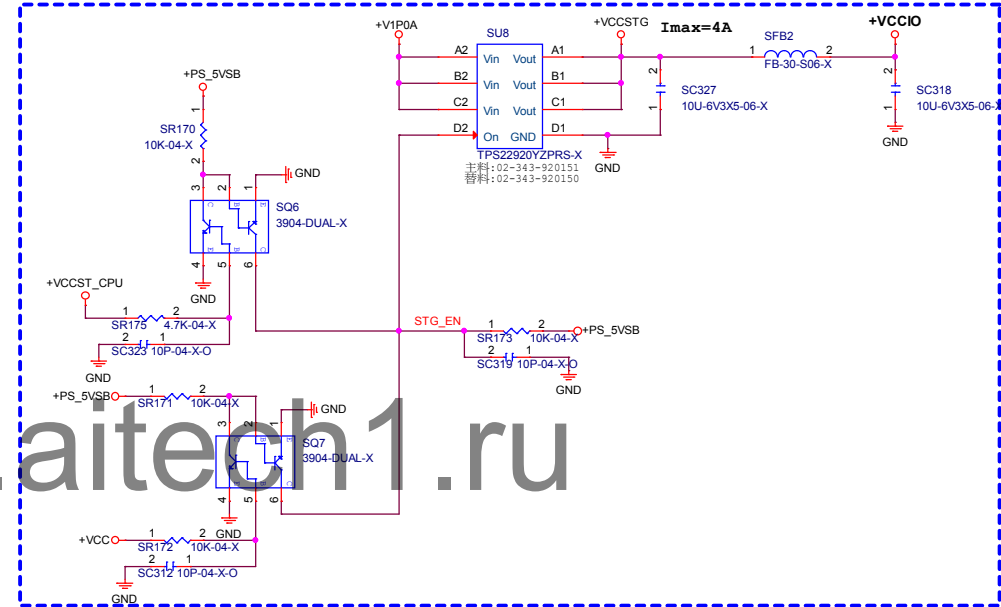
## PCH\_PWROK Sequence



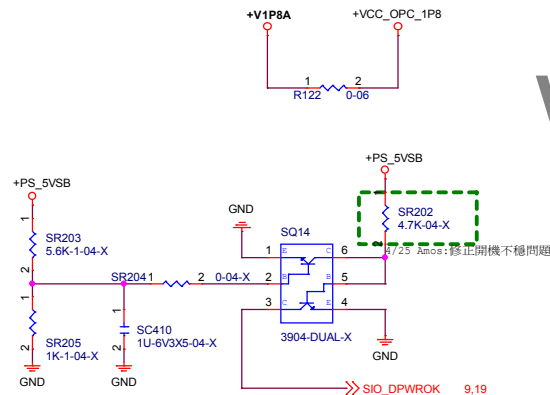
## VCCST\_PWRGD Sequence



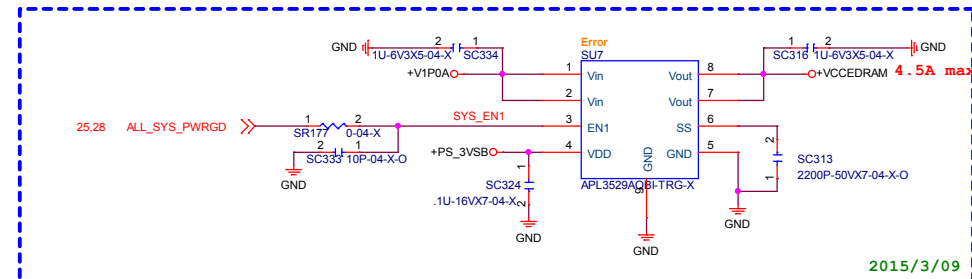
10/19 Amos:機構問題,修改零件



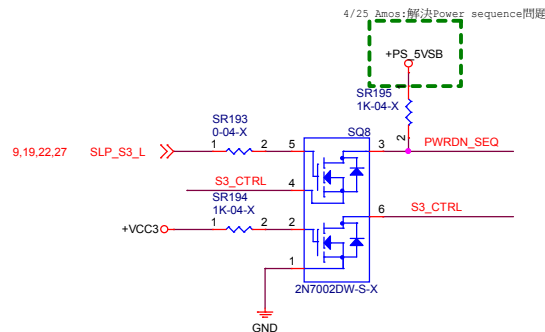
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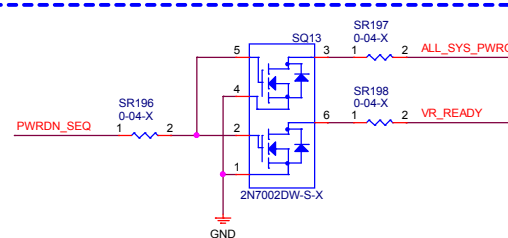
4/25 Amos:修正開機不穩問題

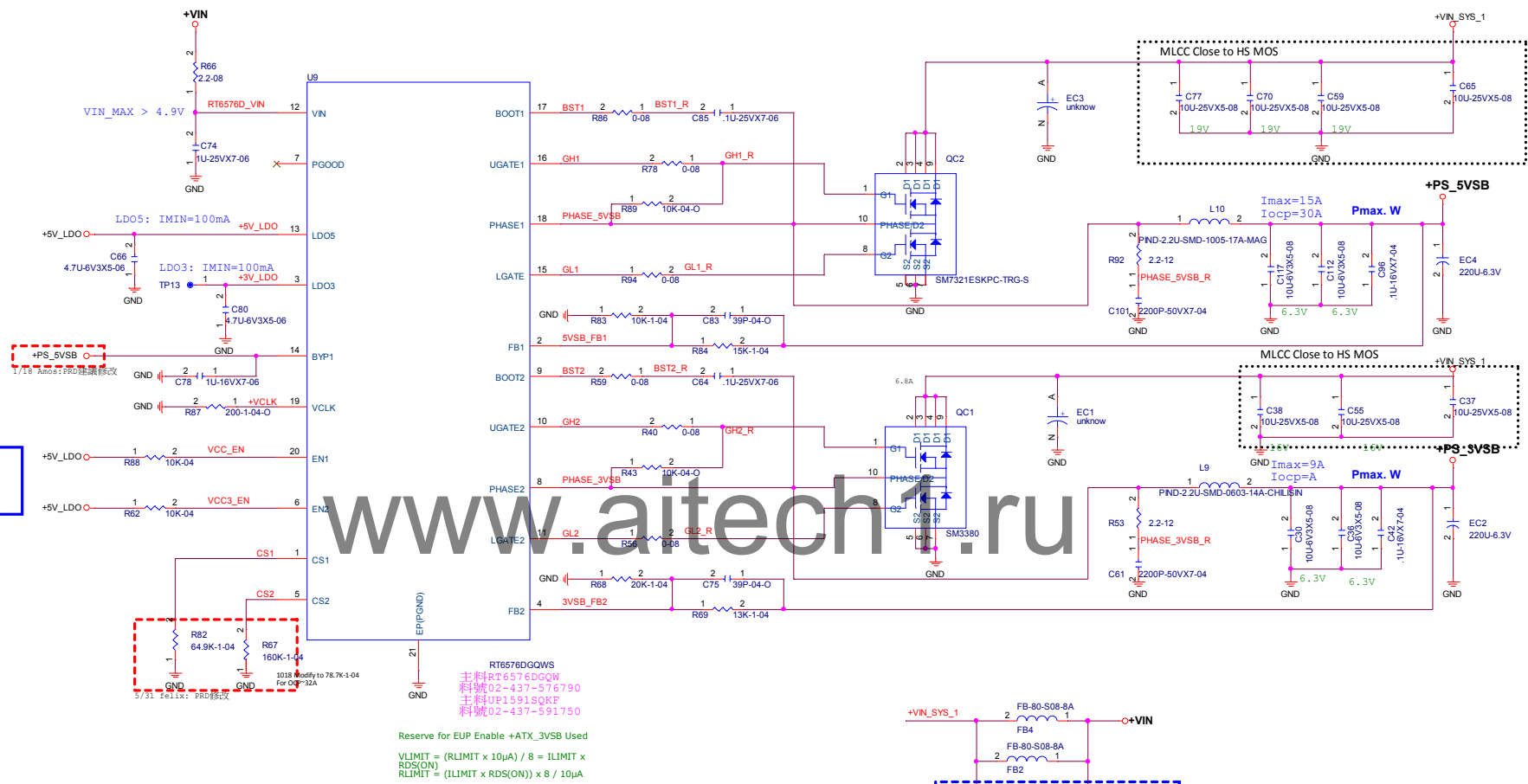


2015/3/09



4/25 Amos:解決Power sequence問題

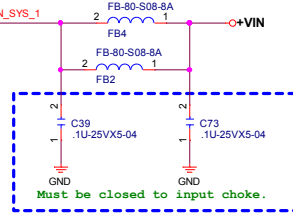




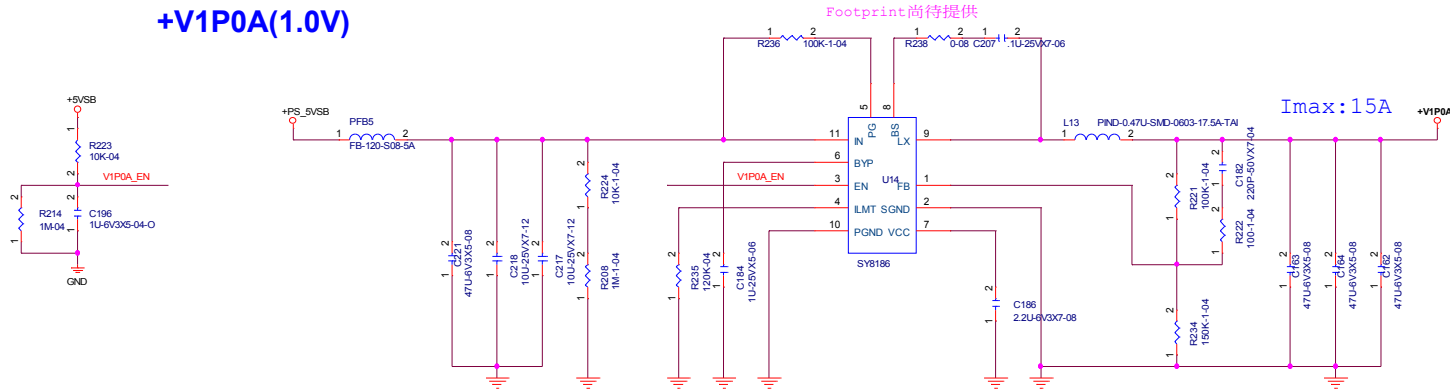
ENX: ON >1.6V  
OFF <0.4V

RT6576DQWS  
主料RT6576DQWS  
料號02-437-576790  
主料UP1591SQKF  
料號02-437-591750

Reserve for EUP Enable +ATX\_3VSB Used  
 $V_{LIMIT} = (R_{LIMIT} \times 10\mu A) / 8 = I_{LIMIT} \times R_{DS(ON)}$   
 $R_{LIMIT} = (I_{LIMIT} \times R_{DS(ON)}) \times 8 / 10\mu A$



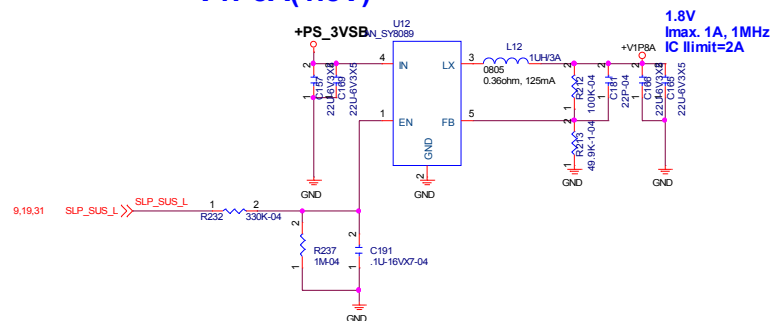
## +V1P0A(1.0V)



VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps

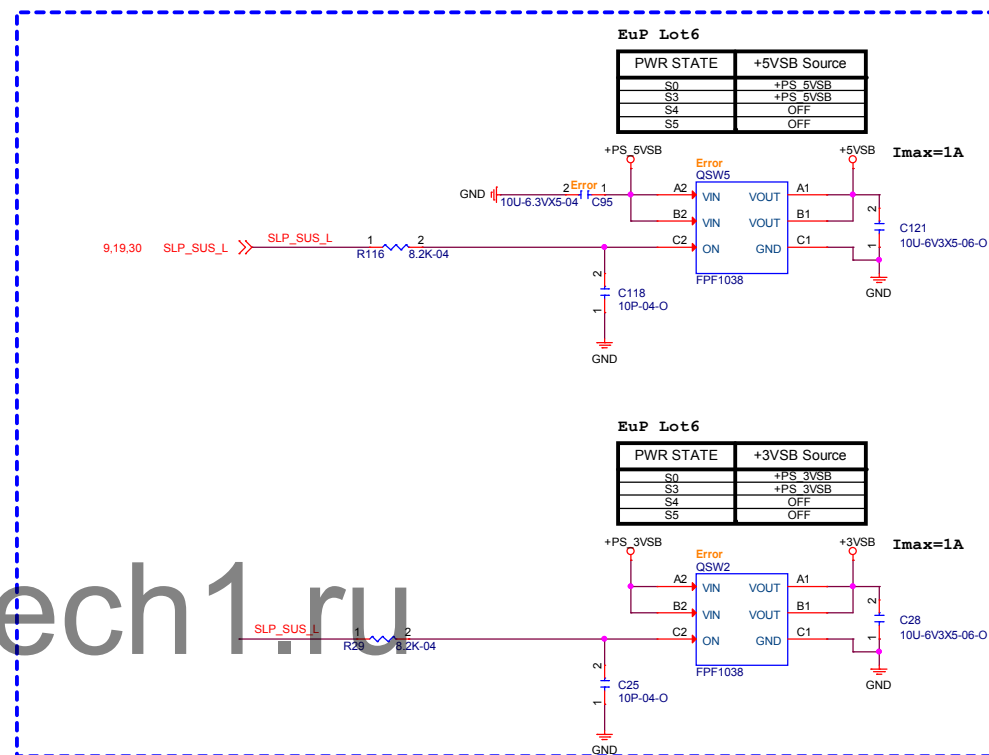
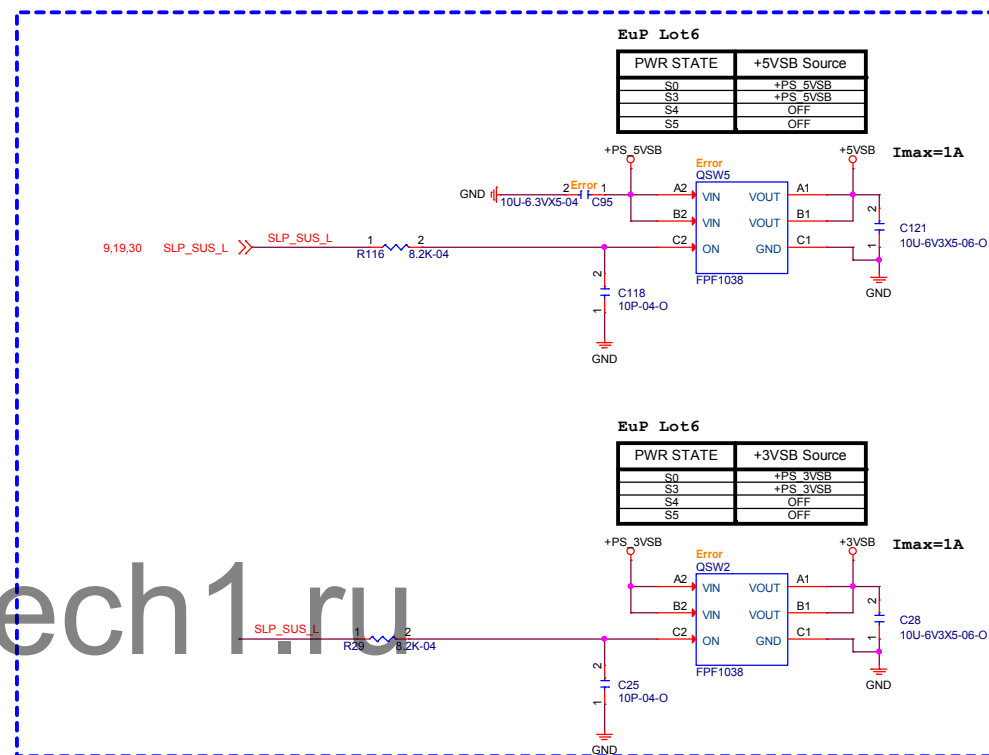
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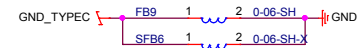
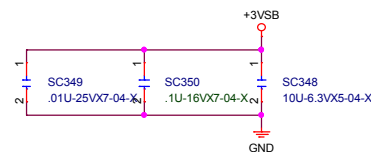
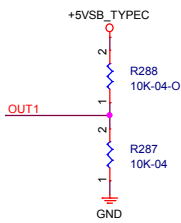
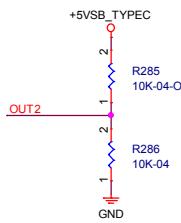
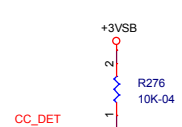
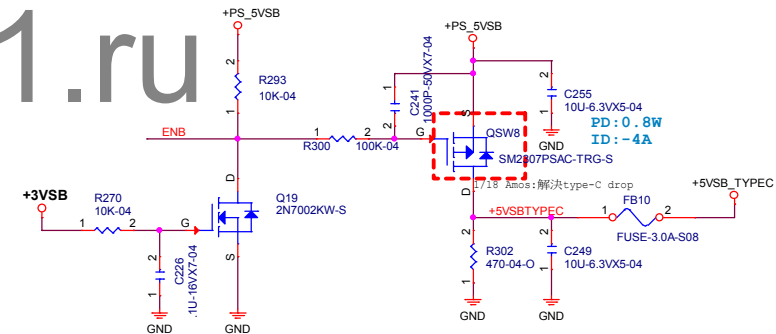
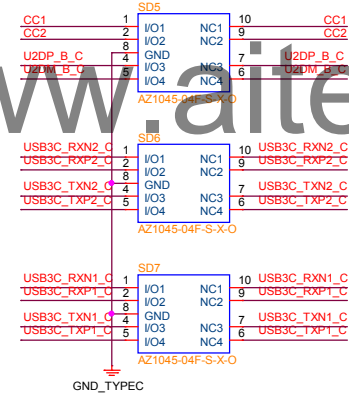
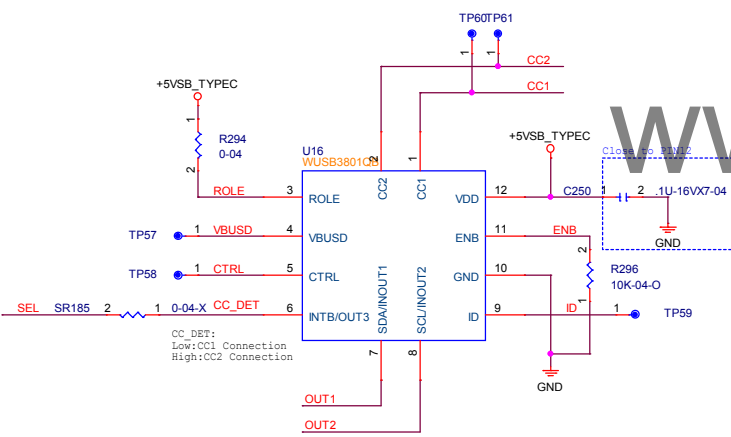
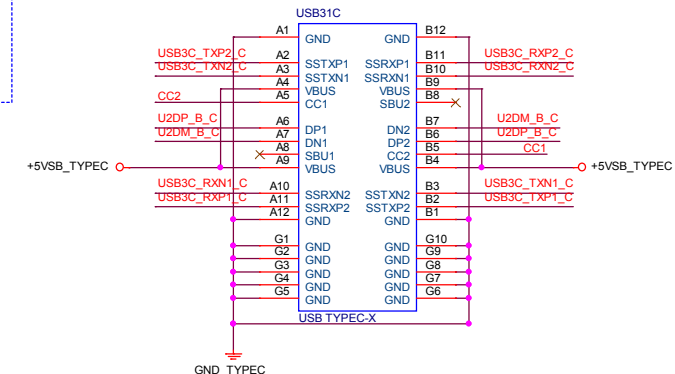
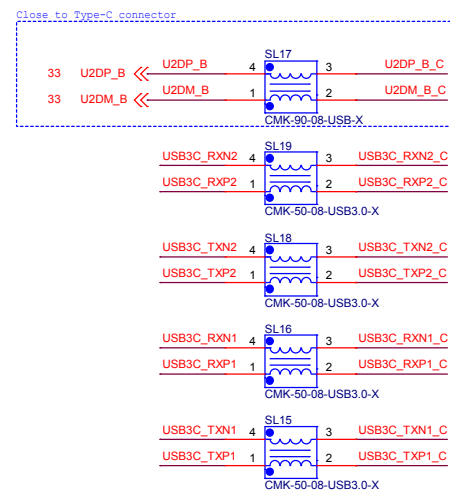
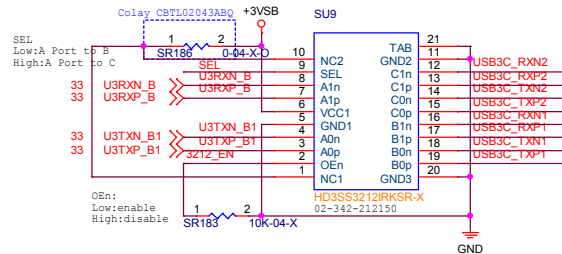
## +V1P8A(1.8V)

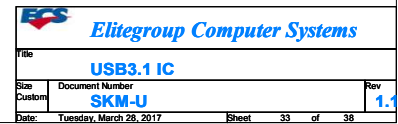


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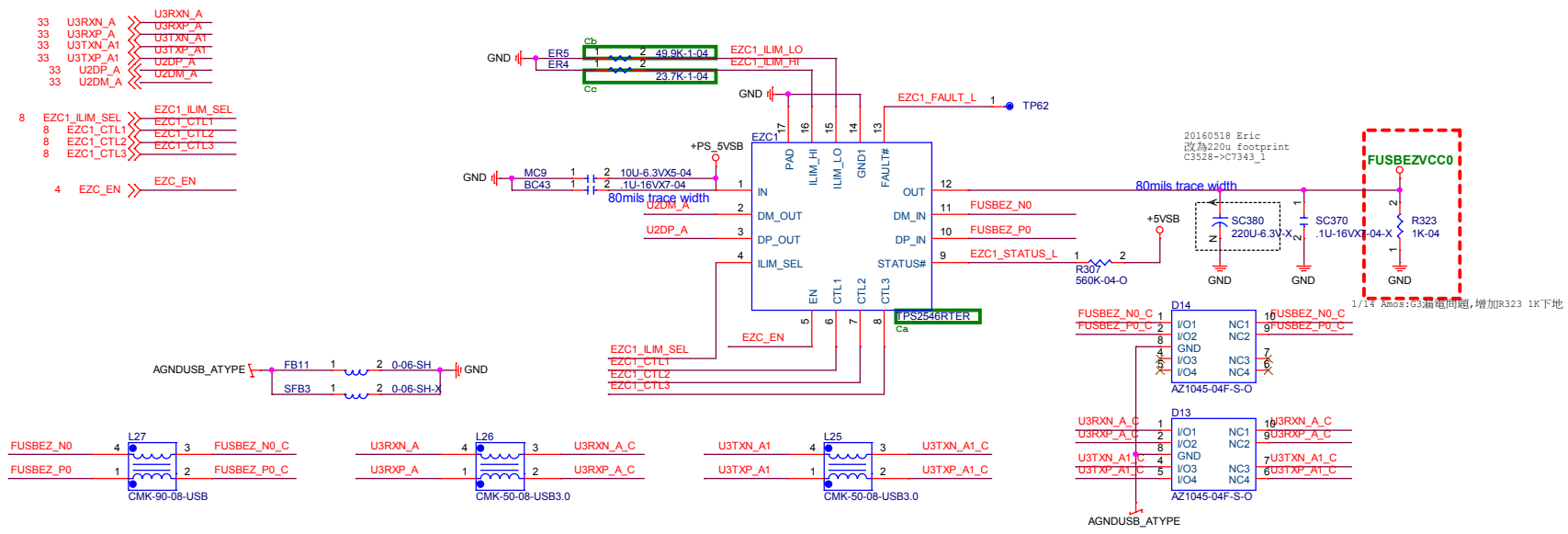
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+V1P0A/+V1P8A			
Size	Document Number	Rev	
Custom	SKM-U	1.1	
Date:	Tuesday, March 28, 2017	Sheet	30 of 38





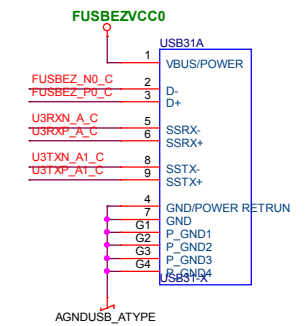






# CO-LAY BOM

Ca	Cb	Cc
TPS2546RTER	49.9K-1-04	23.7K-1-04
VP200	33.2K-1-04	54.7K-1-04

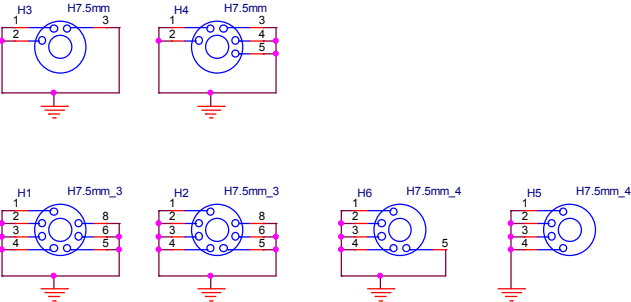
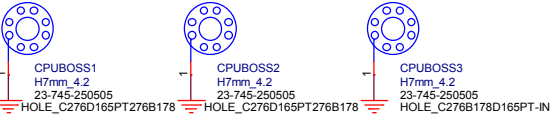



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PCH Strap Pin

Pin Name	Usage	Default Status
SPKR	Top Swap Override	The signal has a weak internal pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default). for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap .
GSPI0_MOSI	No Reboot	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
SMBALERT#	TLS Confidentiality	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
GSPI1_MOSI	Boot BIOS Strap Bit BBS	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCH, bit 6). 0 SPI (Default) 1 LPC
SML0ALERT#	eSPI or LPC	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA	Port B Detected	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected.
DDPC_CTRLDATA	Port C Detected	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected.

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Title <b>104/STRAPPING</b>		
Size Custom	Document Number <b>SKM-U</b>	Rev 1.1
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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status	Bios Set
GPP_B16	3VSB	GPP_B16(BIOS override)	GPI	GPO(Hi)
GPP_A18	3VSB	BIOS_CONFIG	GPI	GPI
GPP_A19	3VSB	GPP_A19(BIOS Config)	GPI	GPI
GPP_B20	DSW	PWR_LED	GPI	GPO(Hi)
GPP_B17	+V_3P3_LAN	WLAN_DISABLE_L	GPI	GPO(Hi)
GPP_C8	3VSB	USB_charger EN	GPI	GPO(Hi)
GPP_C21	VCC3	LOGO_LED	GPI	GPO(Low)
GPP_C22	VCC3	USB3.1 SMI	GPI	SMI(follow Z170-claymore)
GPP_C23	3VSB	USB3.1 WAKE	GPI	GPI
GPP_C18	+V_3P3_LAN	M.2 ALERT	GPI	GPI
GPP_B3	+V_3P3_LAN	BT_DISABLE	GPI	GPO
GPP_D9	VCC3	HDMI_ENABLE	GPI	GPO(Low)
GPP_D19	3VSB	ILM_SEL	GPI	GPO(follow Z170-claymore)
GPP_D20	3VSB	CTL1	GPI	GPO(follow Z170-claymore)
GPP_D17	3VSB	CTL2	GPI	GPO(follow Z170-claymore)
GPP_D18	3VSB	CTL3	GPI	GPO(follow Z170-claymore)
GPP_D2	VCC3	BOM select	GPI	GPI
GPP_D3	VCC3	BOM select	GPI	GPI
GPP_D0	VCC3	BOM select	GPI	GPI
GPP_D21	VCC3	BOM select	GPI	GPI
GPP_D22	VCC3	BOM select	GPI	GPI


SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP22	PS_5VSB	PWR_LED(S0=>low , S3=>blinking)	

PCH-INT Function

Function	INT Port	PCIE_X1 Port	Device
LAN Ethernet Controller	INT B#	PE_TX/RX_4	LAN-I219V
AC-8260(M.2)_WLAN	INT A#	PE_TX/RX_5	AC_8260
PCIE_M.2(22x80)	INT A#	PE_TX/RX_9	PCIE_M.2
SATA Controller	INT C#	N/A	SATA

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 <h1 style="display: inline; margin-left: 10px;">Elitegroup Computer Systems</h1>			
Title			
<h2>Power Sequence</h2>			
Size Custom	Document Number		Rev
	<h2>SKM-U</h2>		1.1
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